

Figure 1

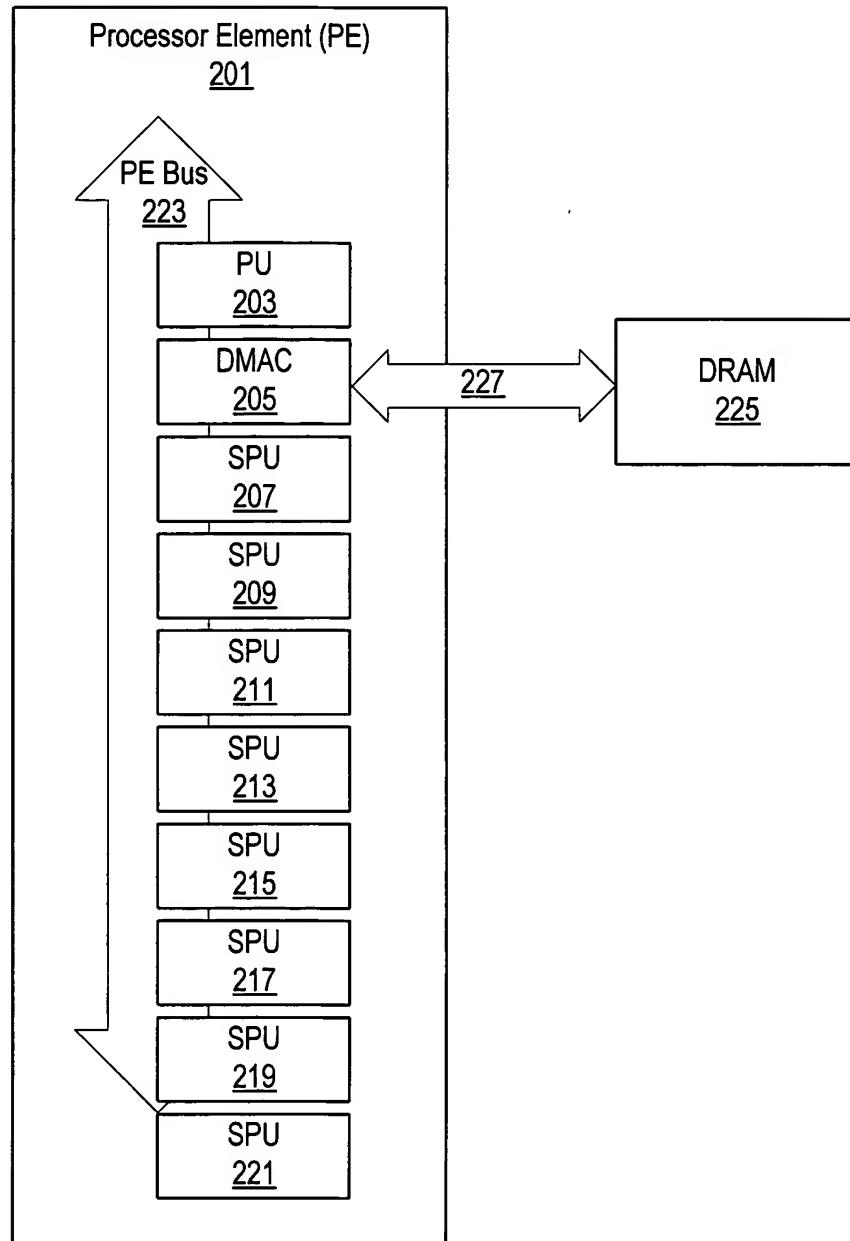


Figure 2

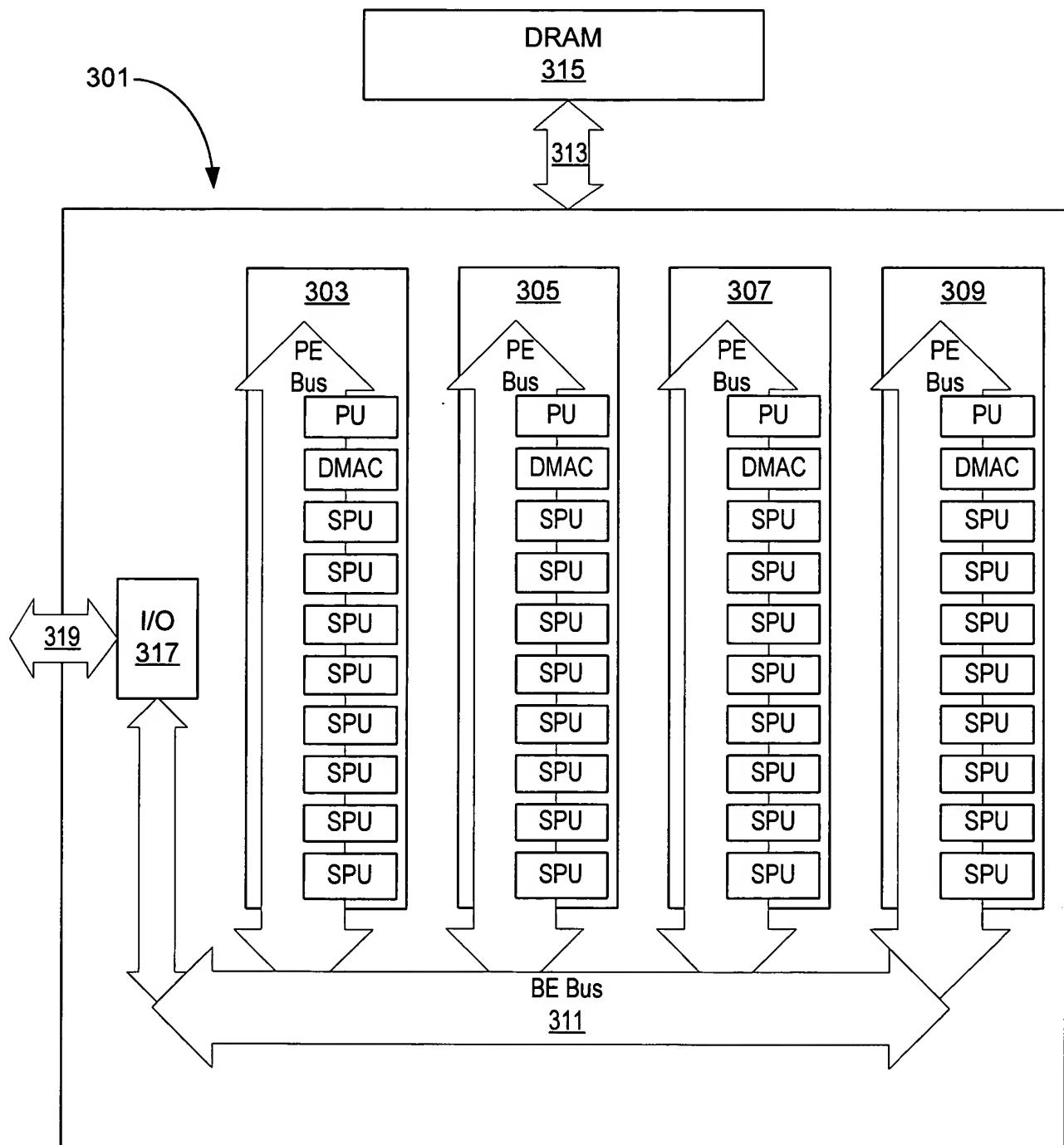


Figure 3

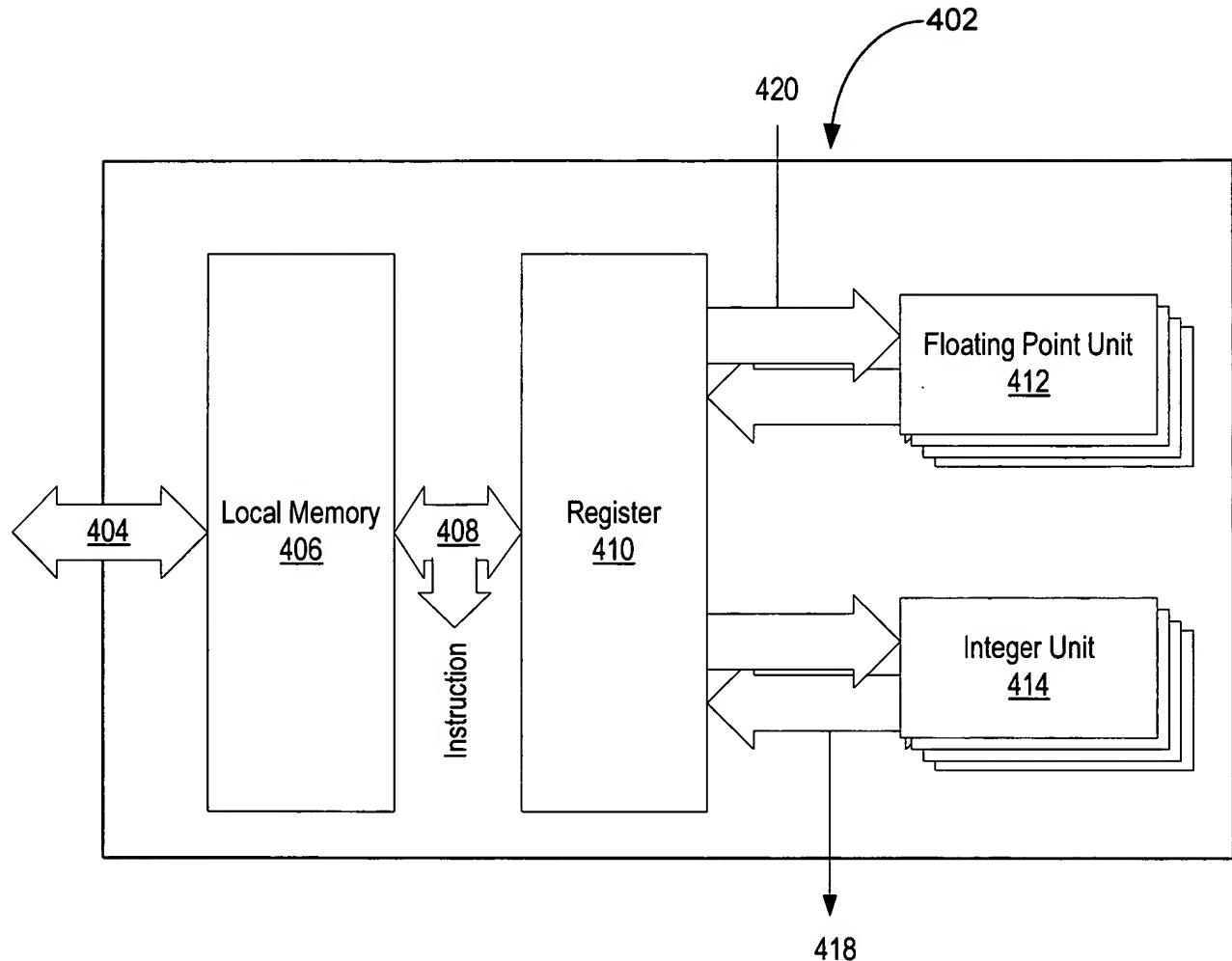


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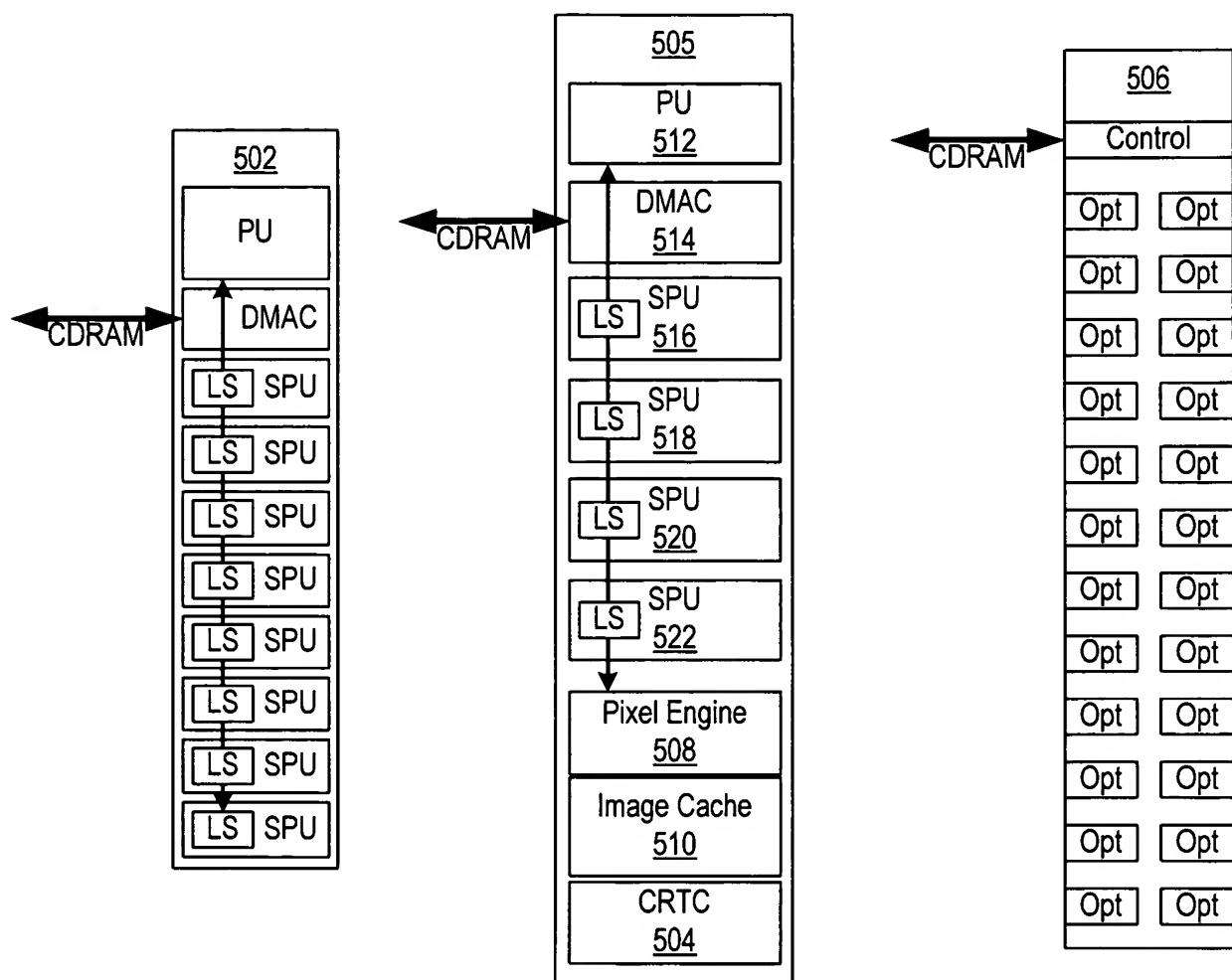


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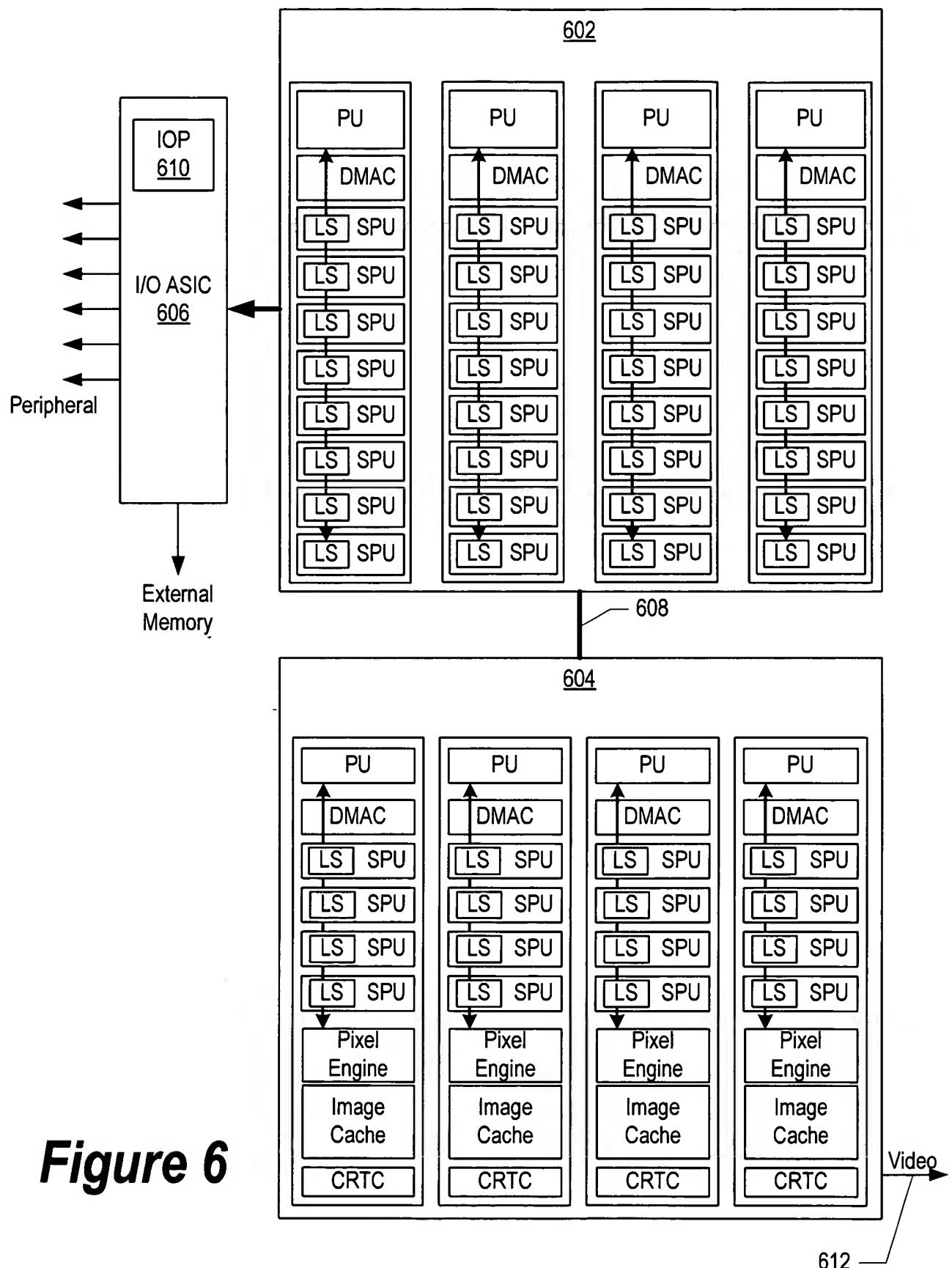


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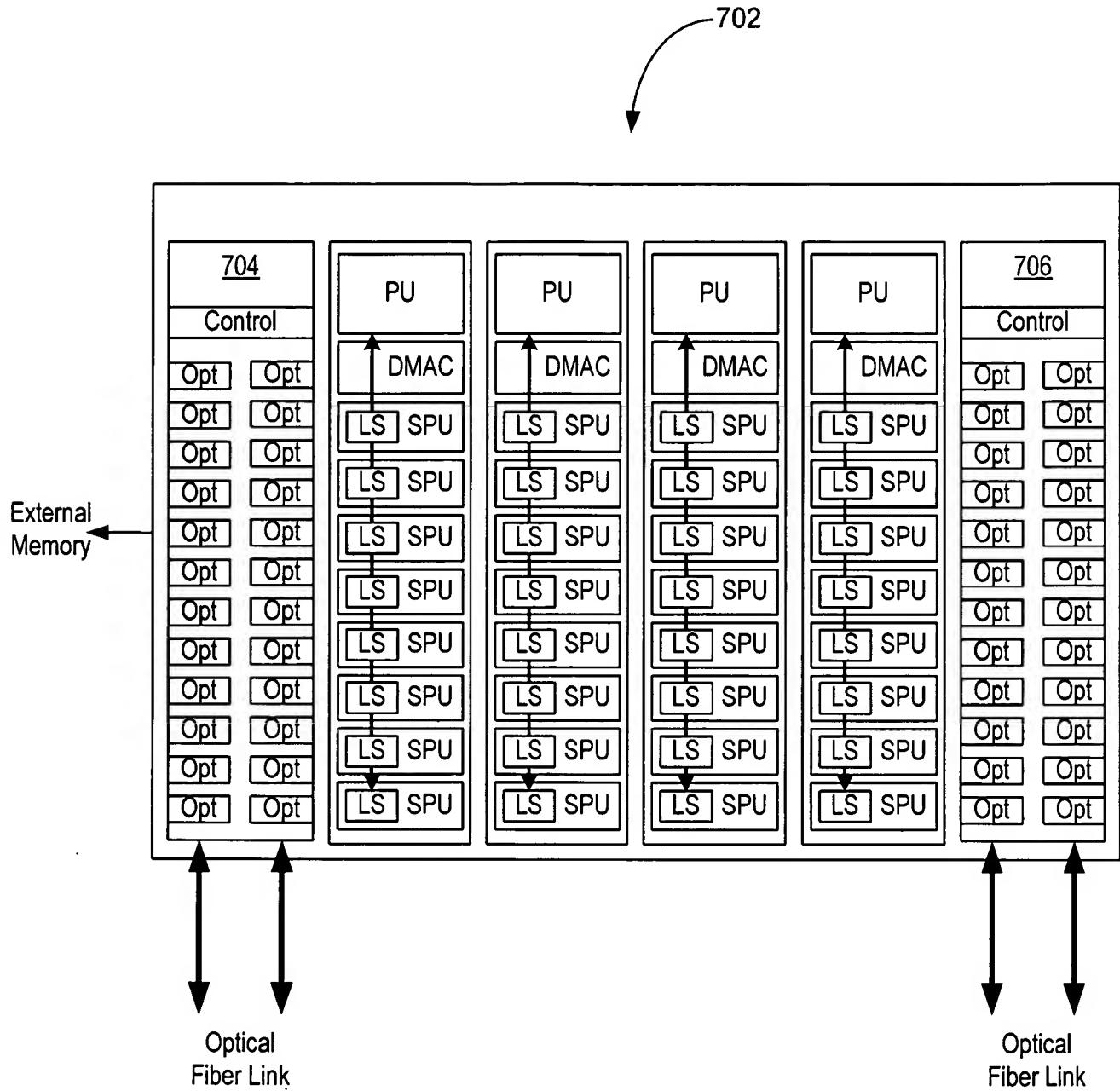


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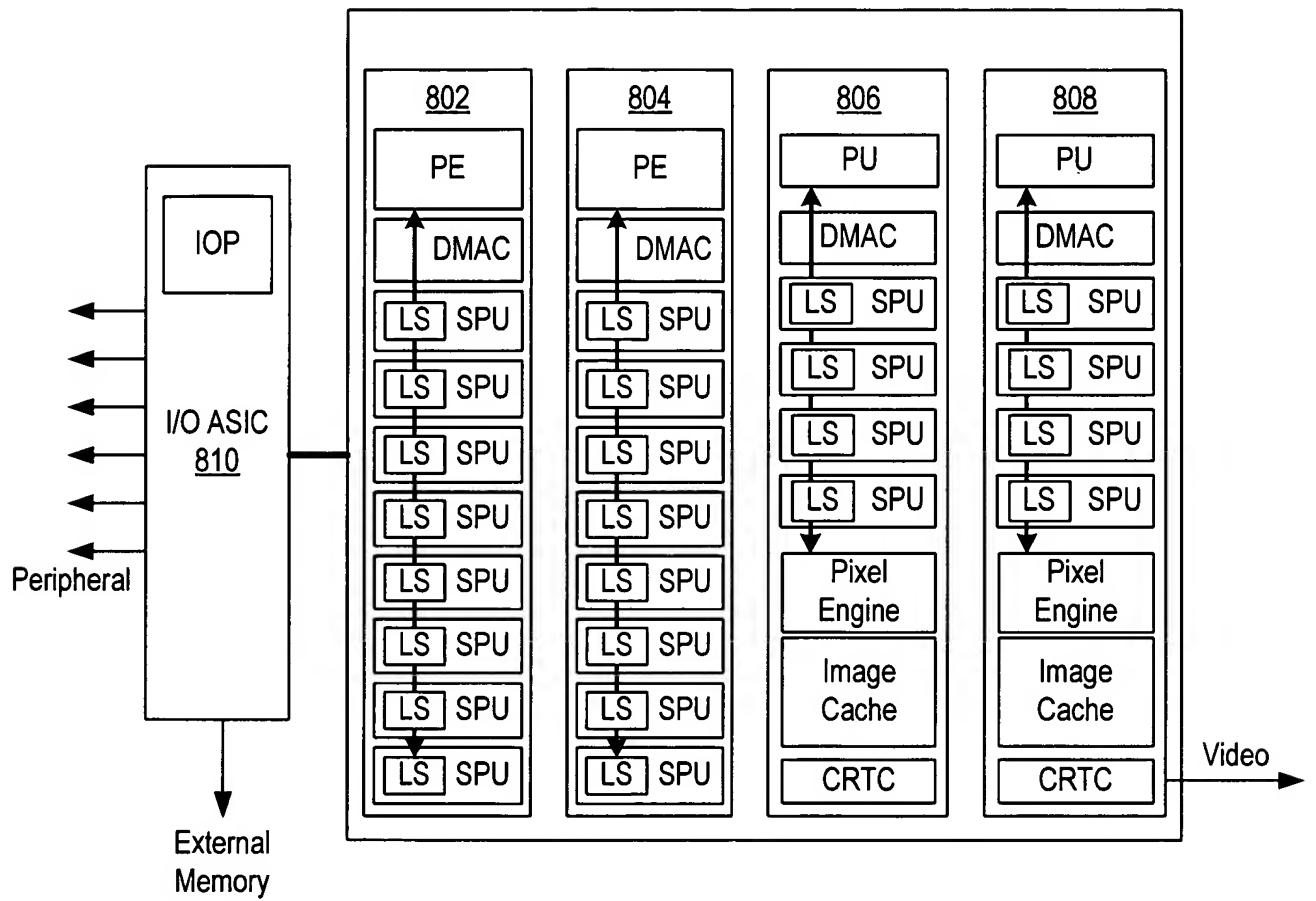


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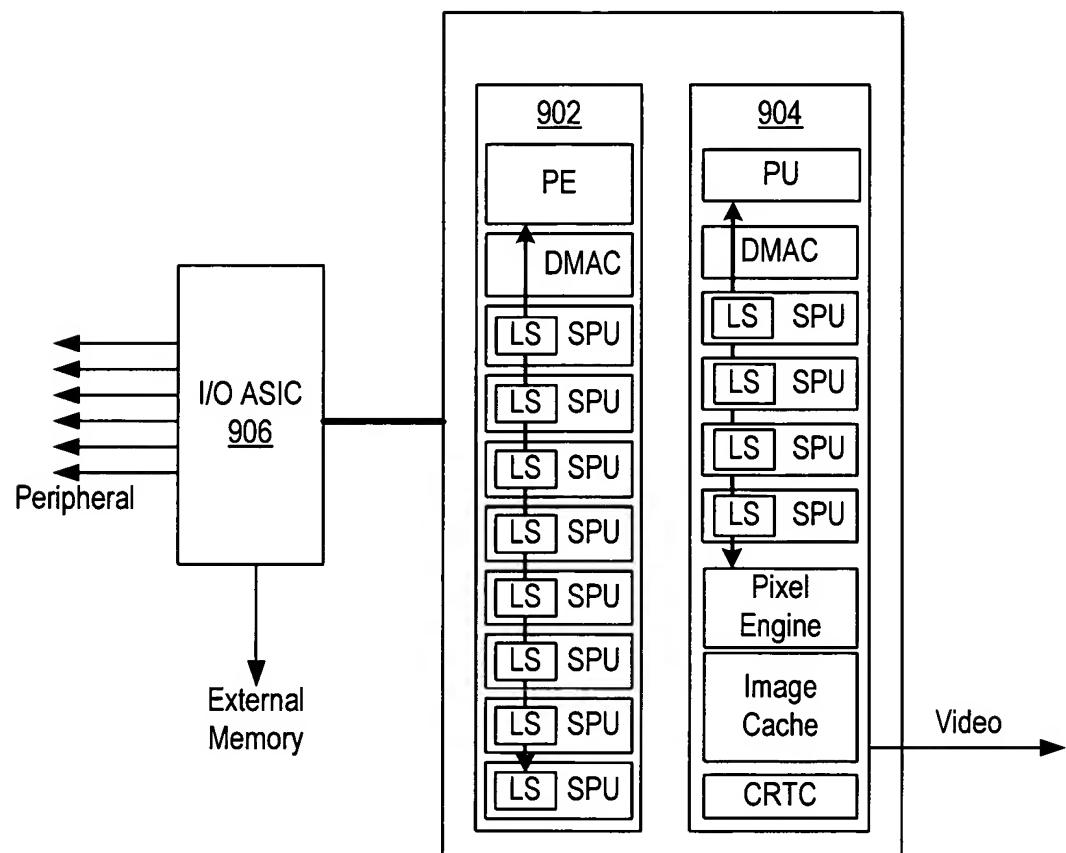


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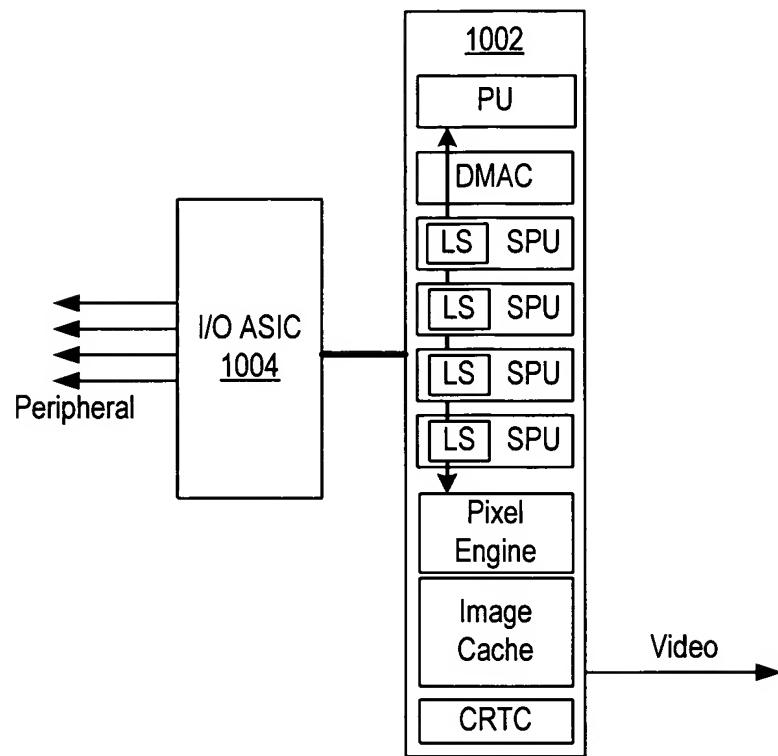
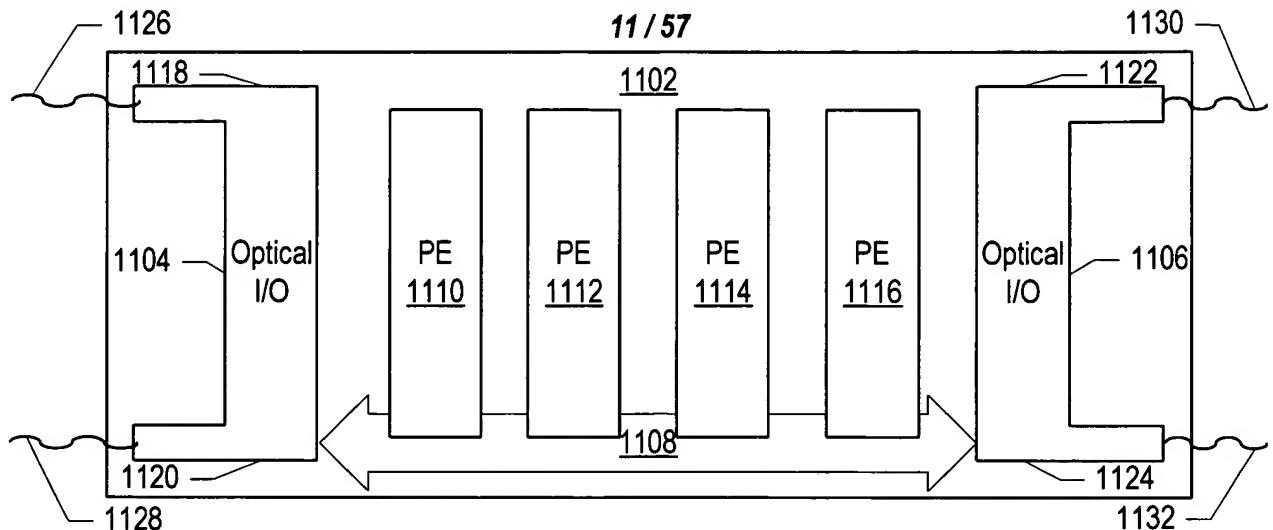
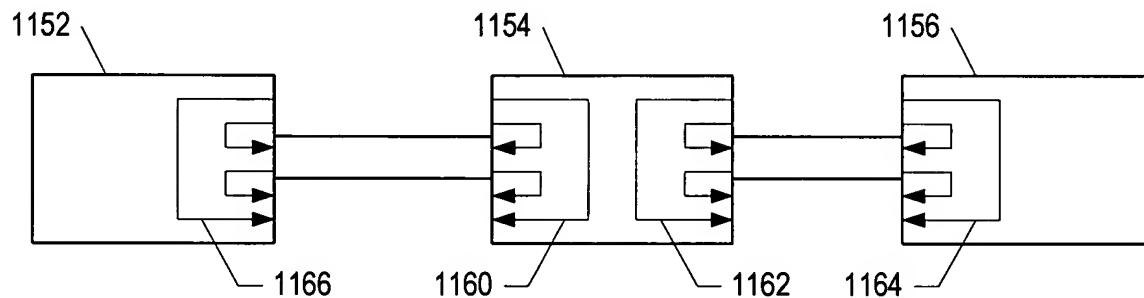
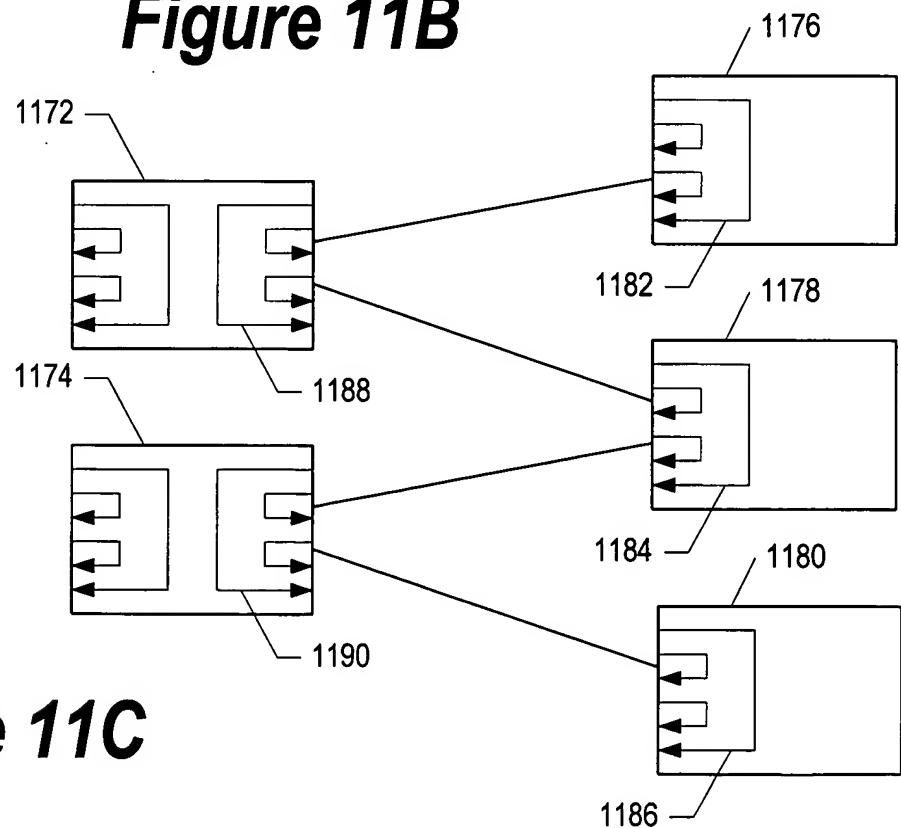


Figure 10

**Figure 11A****Figure 11B****Figure 11C**

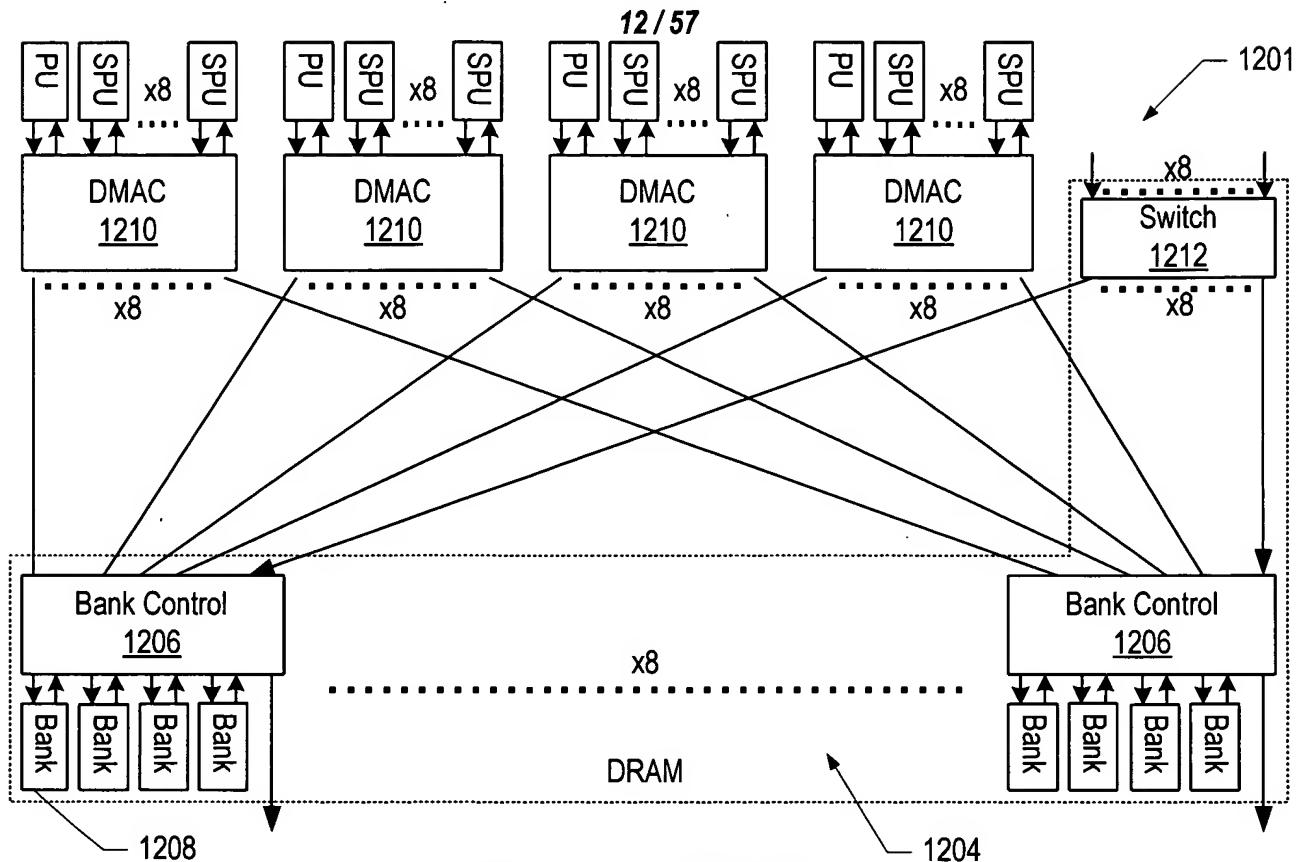


Figure 12A

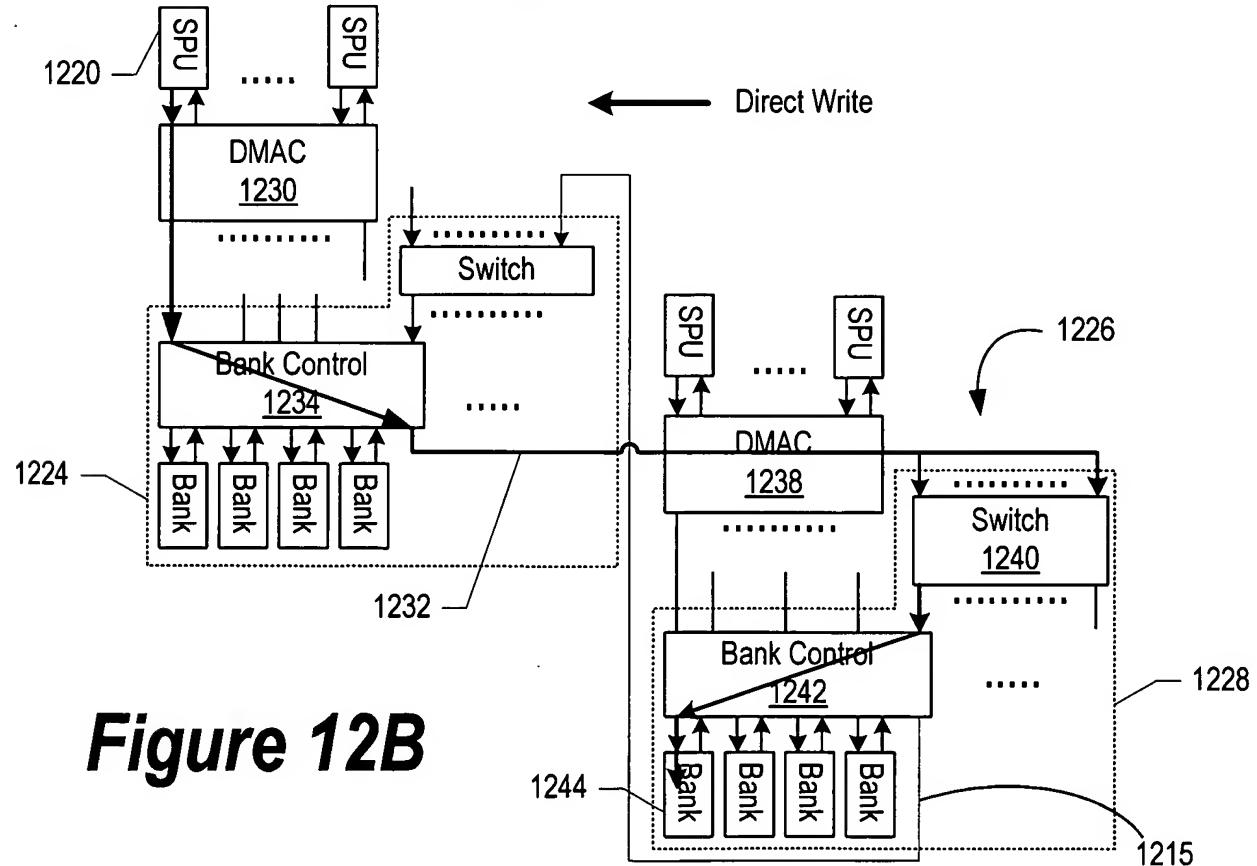


Figure 12B

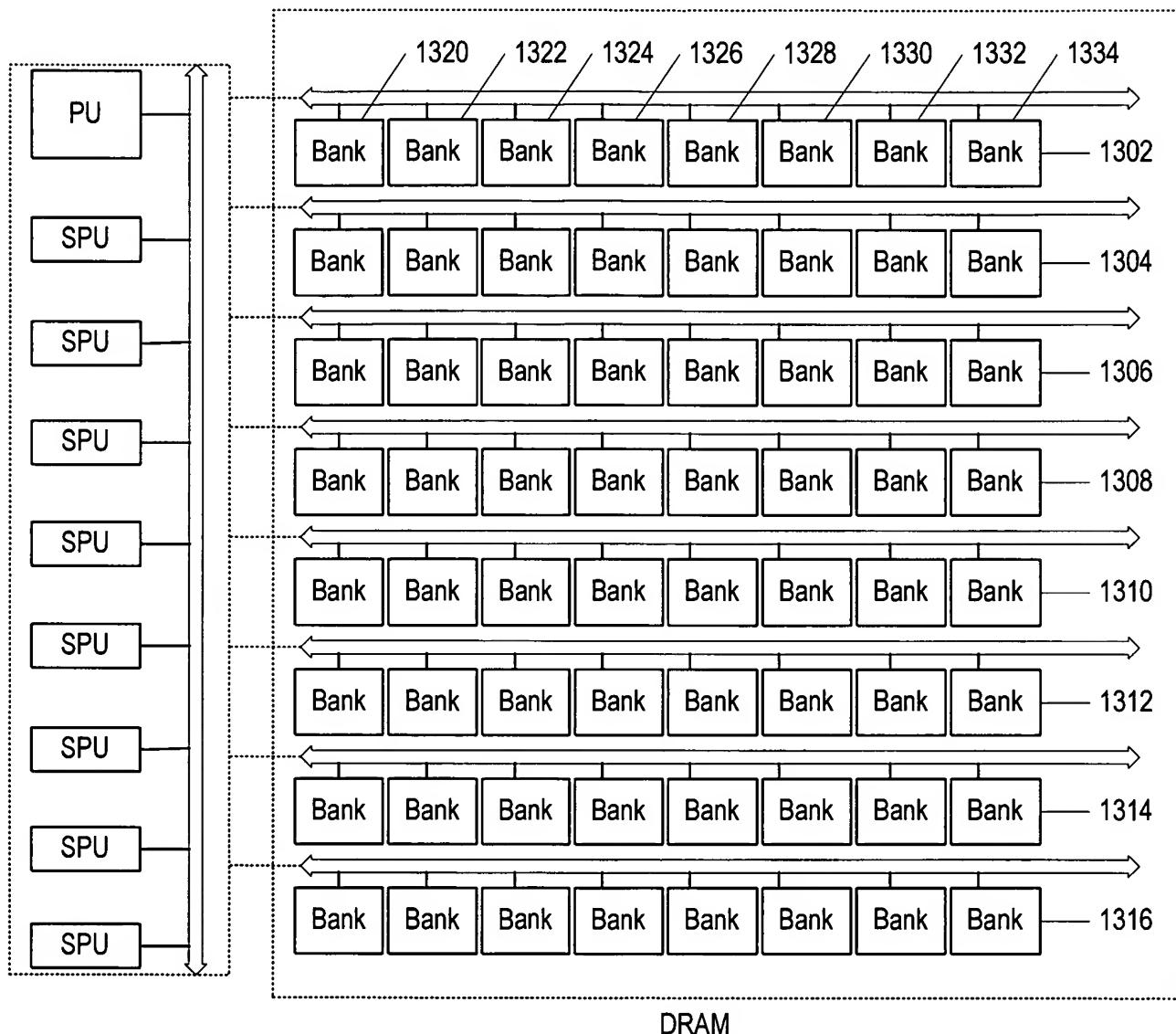


Figure 13

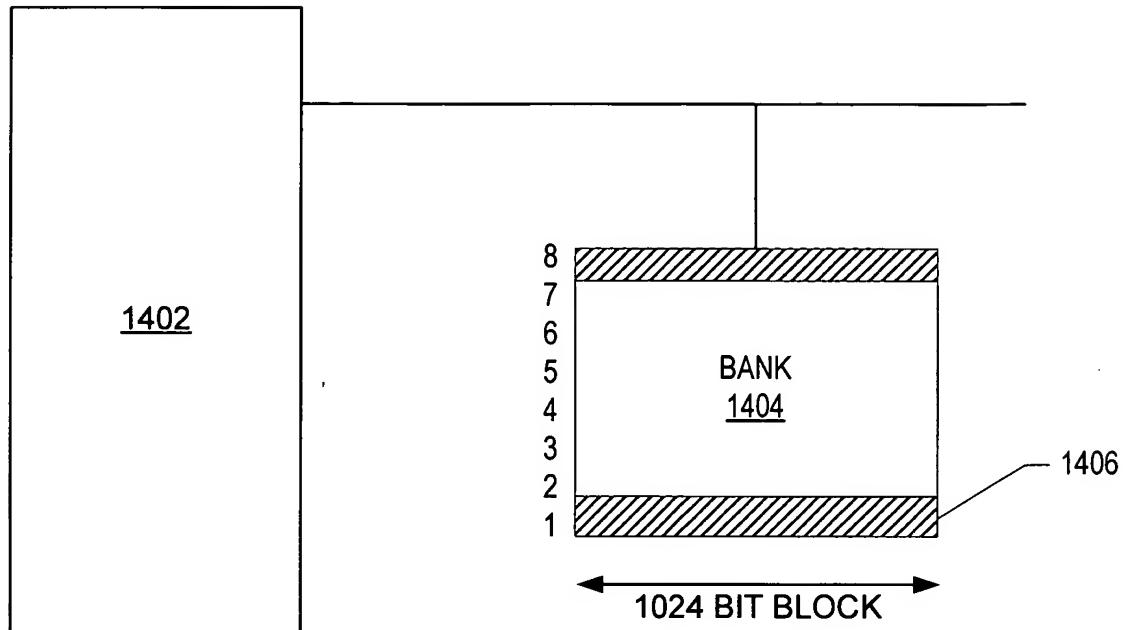


Figure 14A

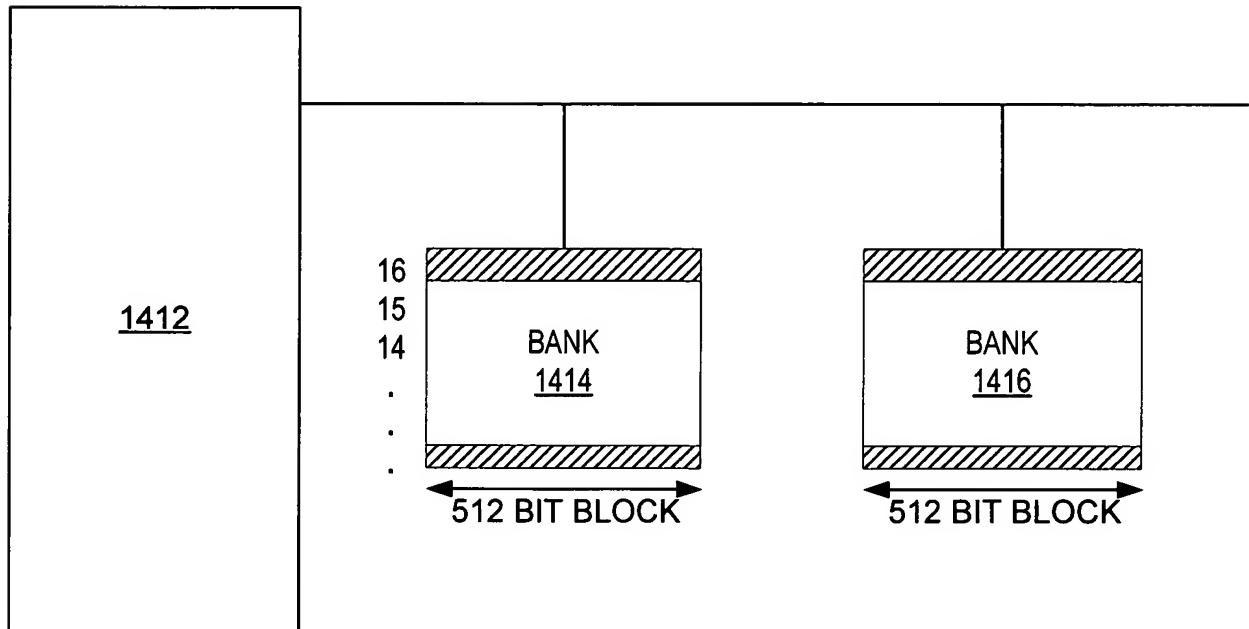


Figure 14B

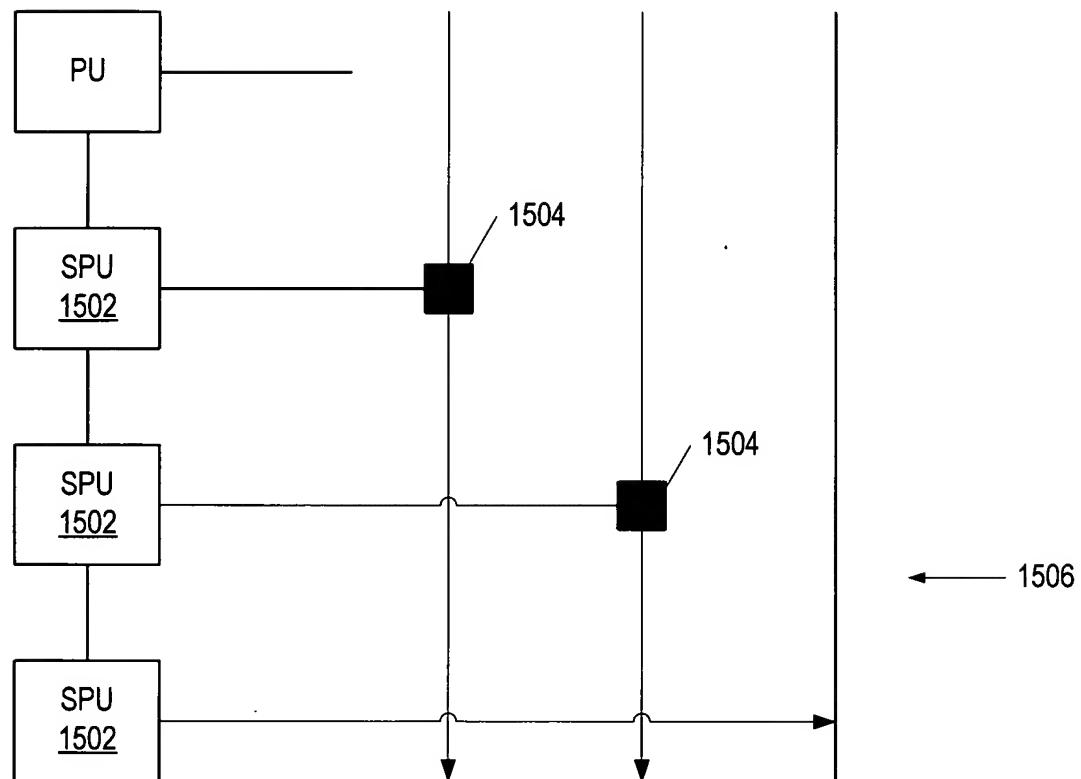


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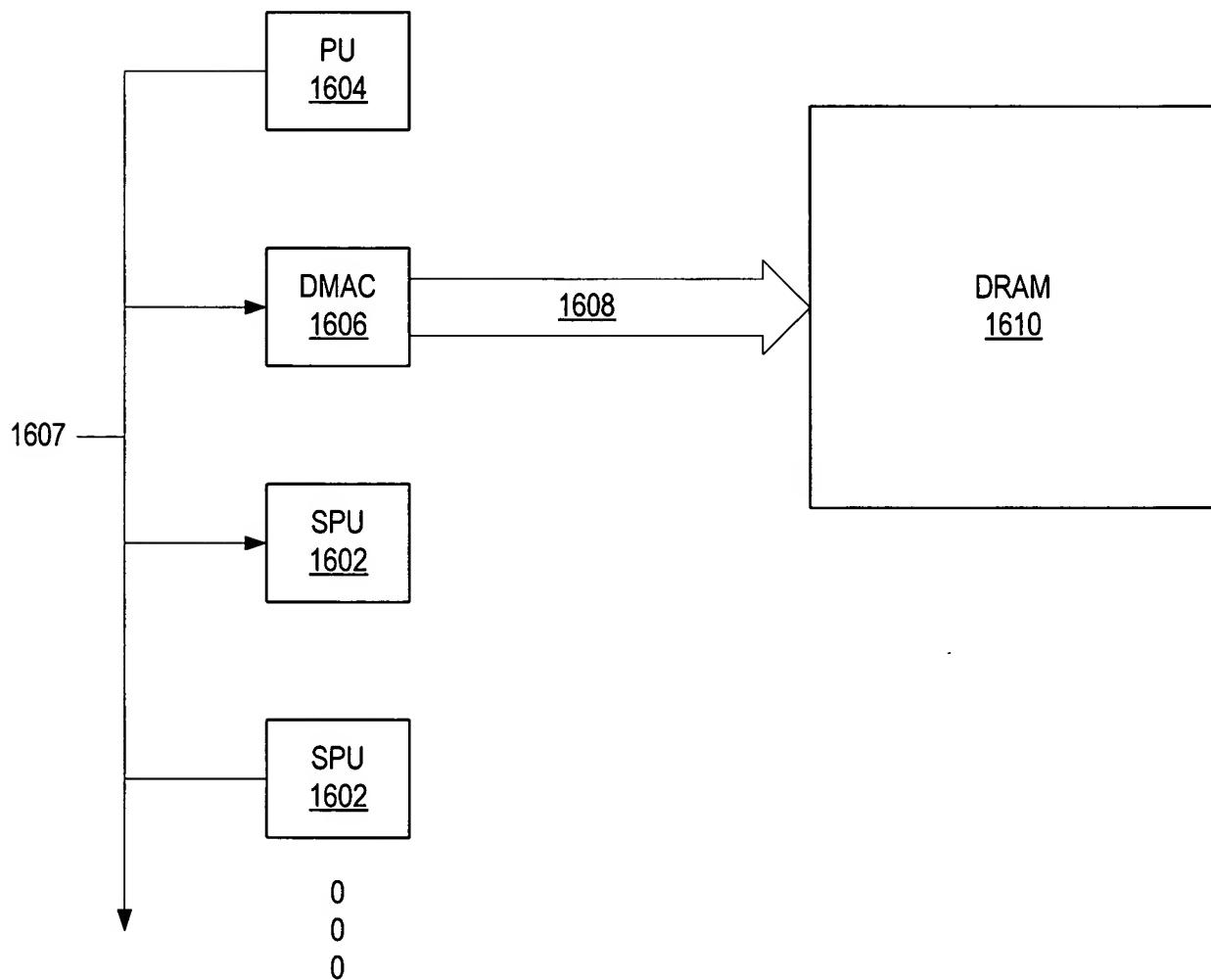


Figure 16

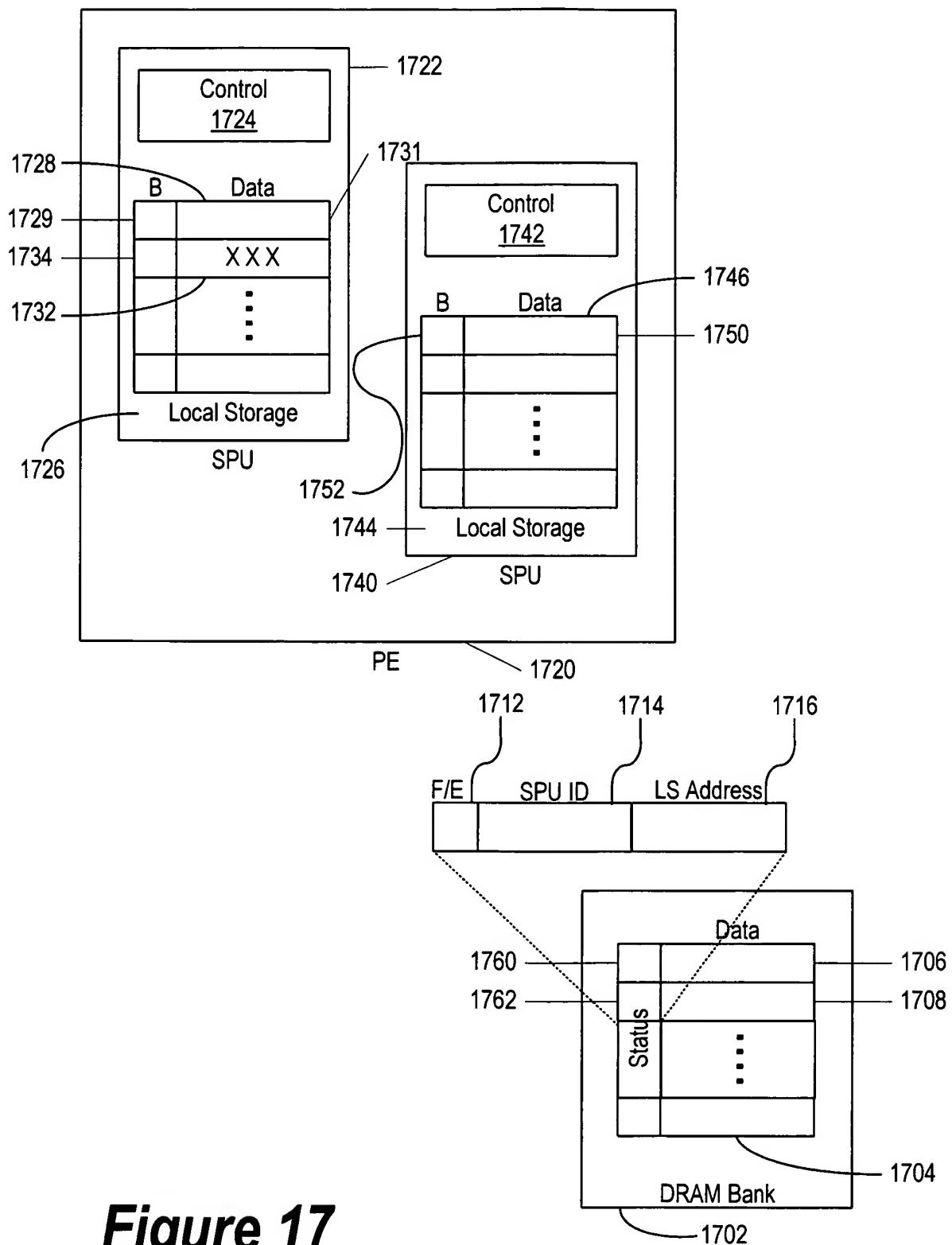


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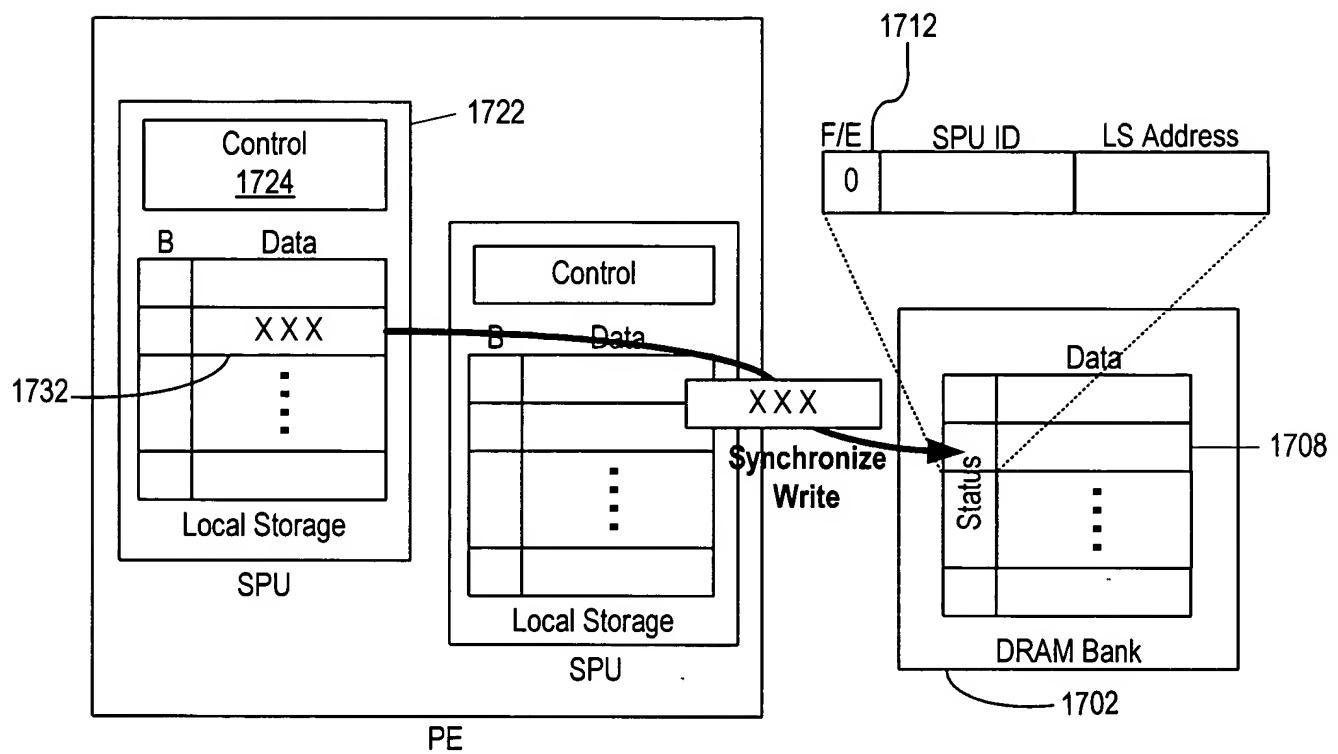


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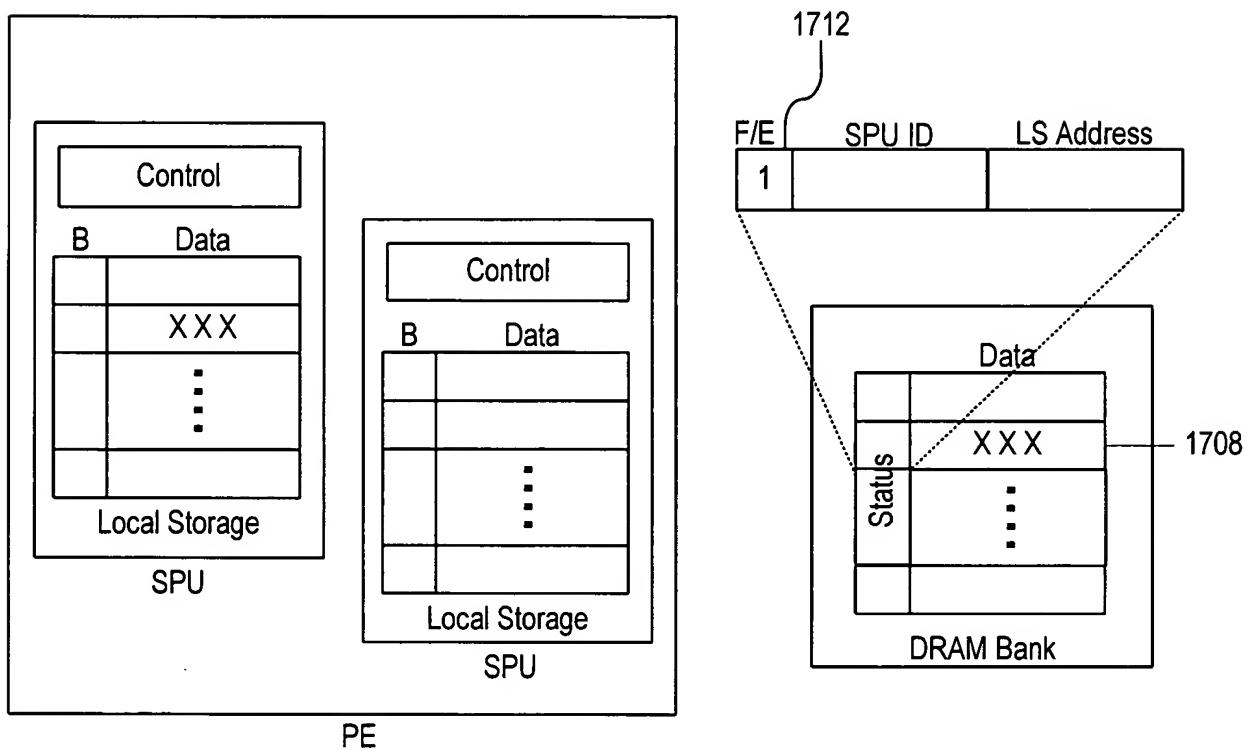


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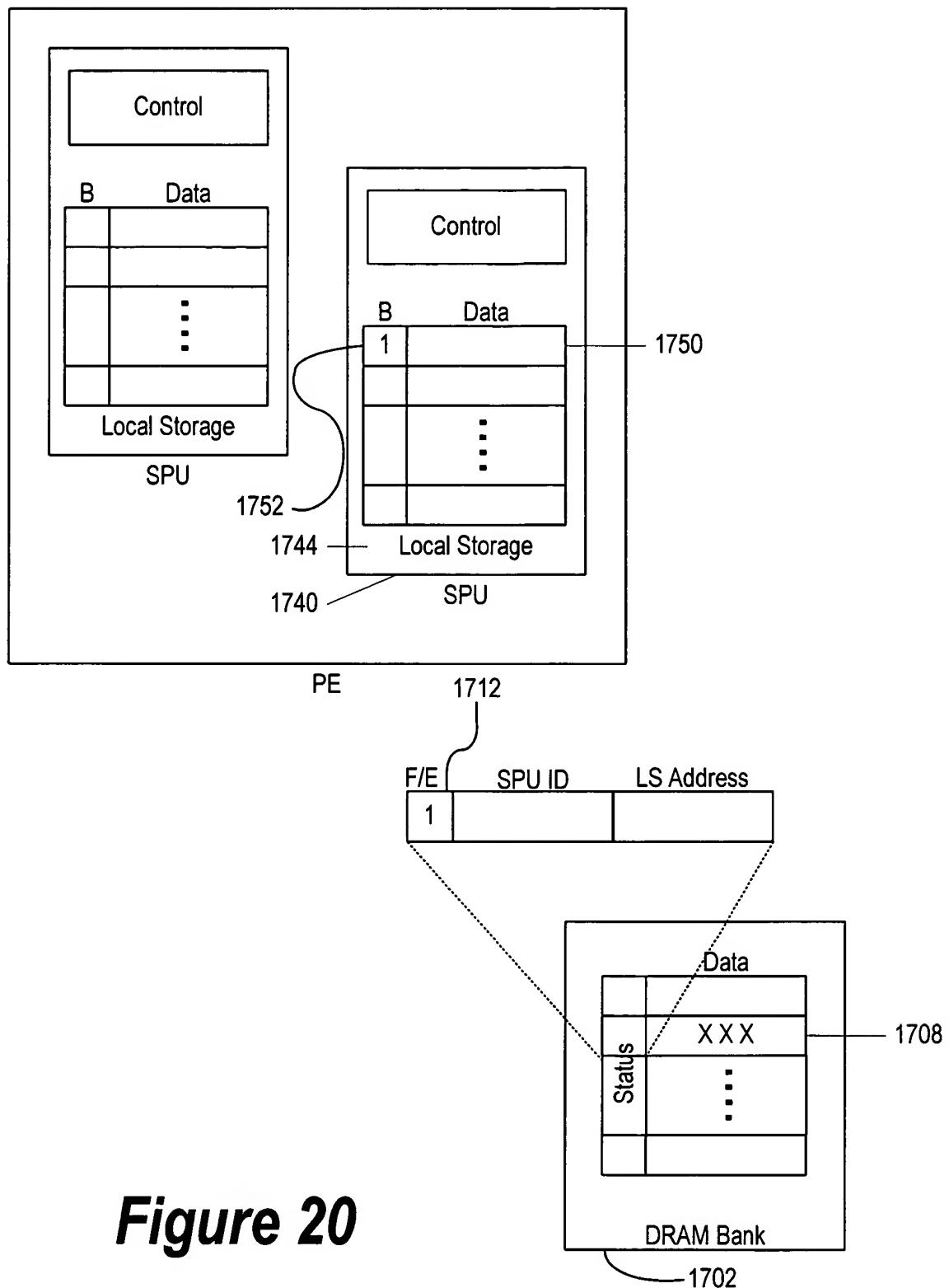


Figure 20

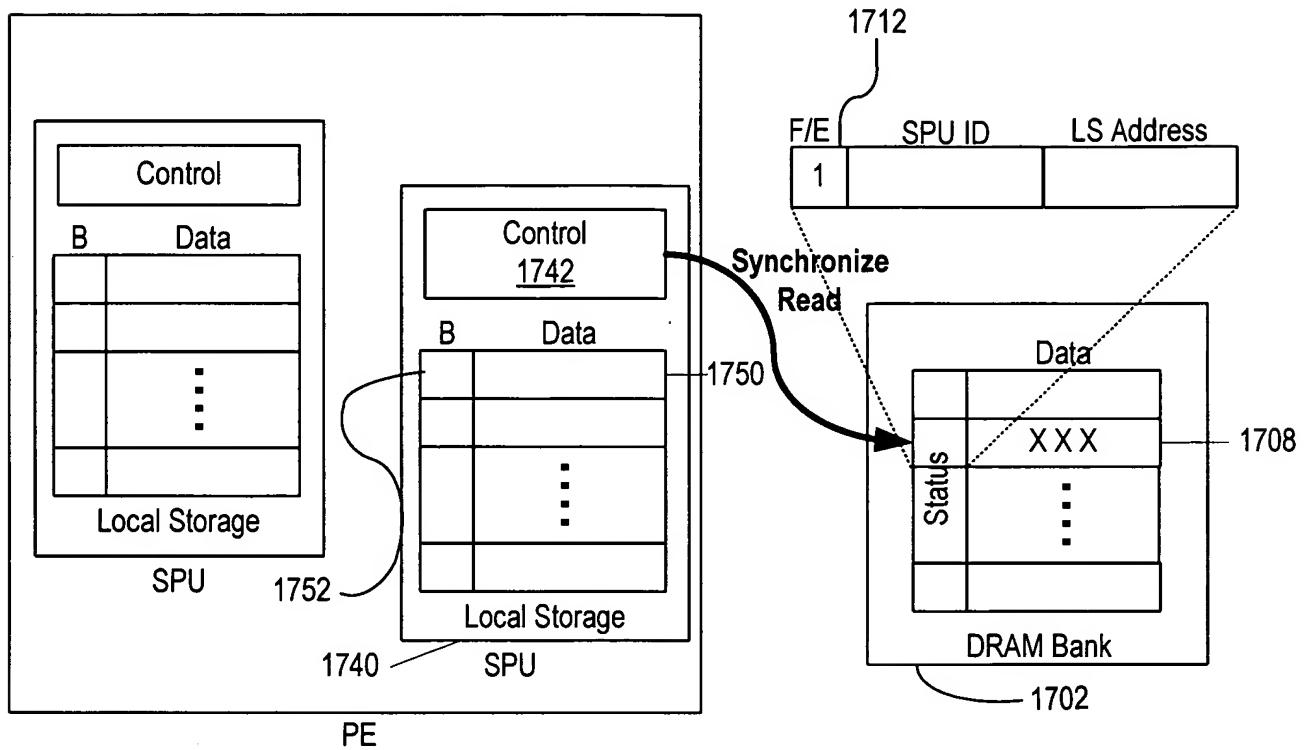


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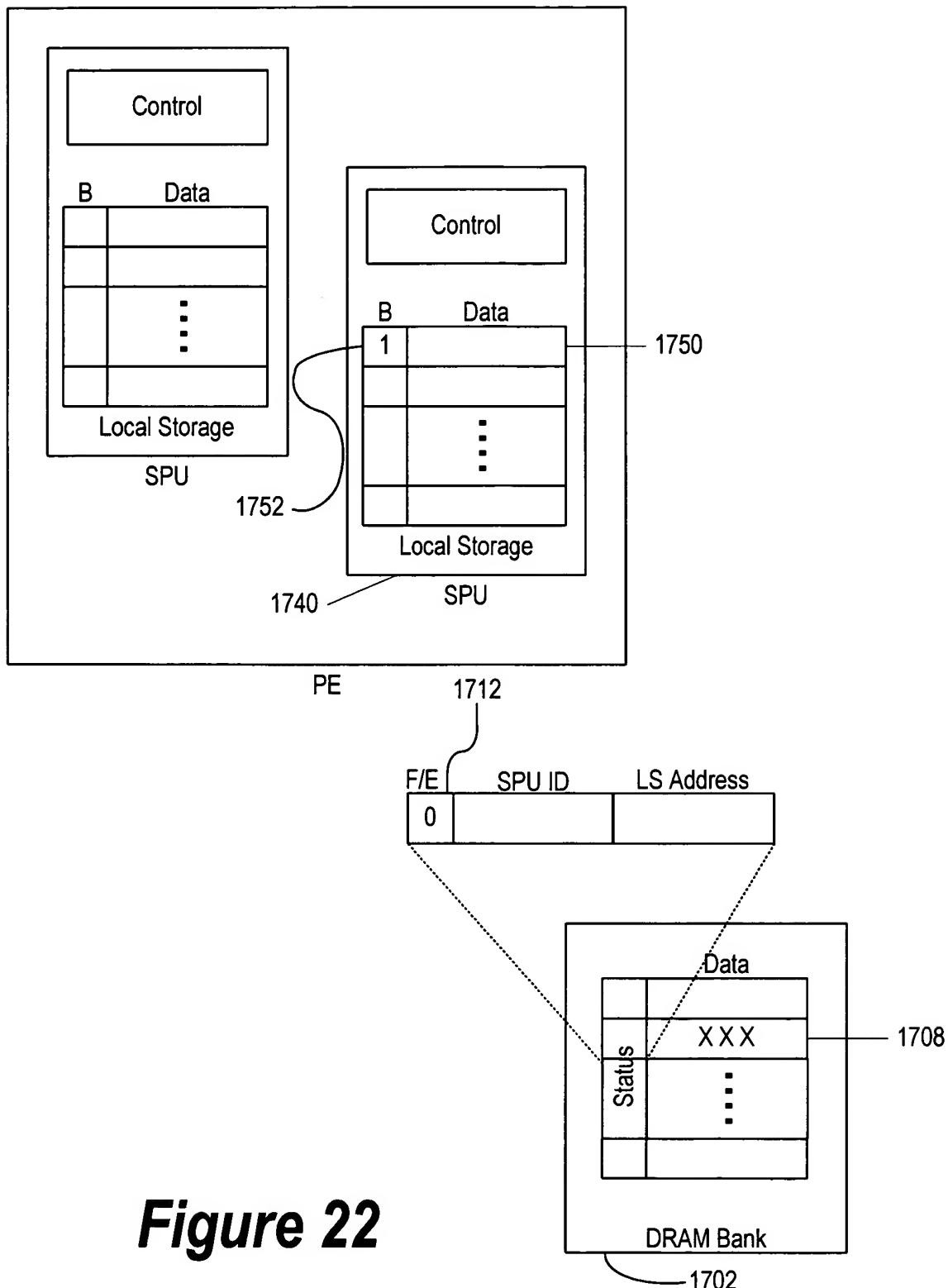


Figure 22

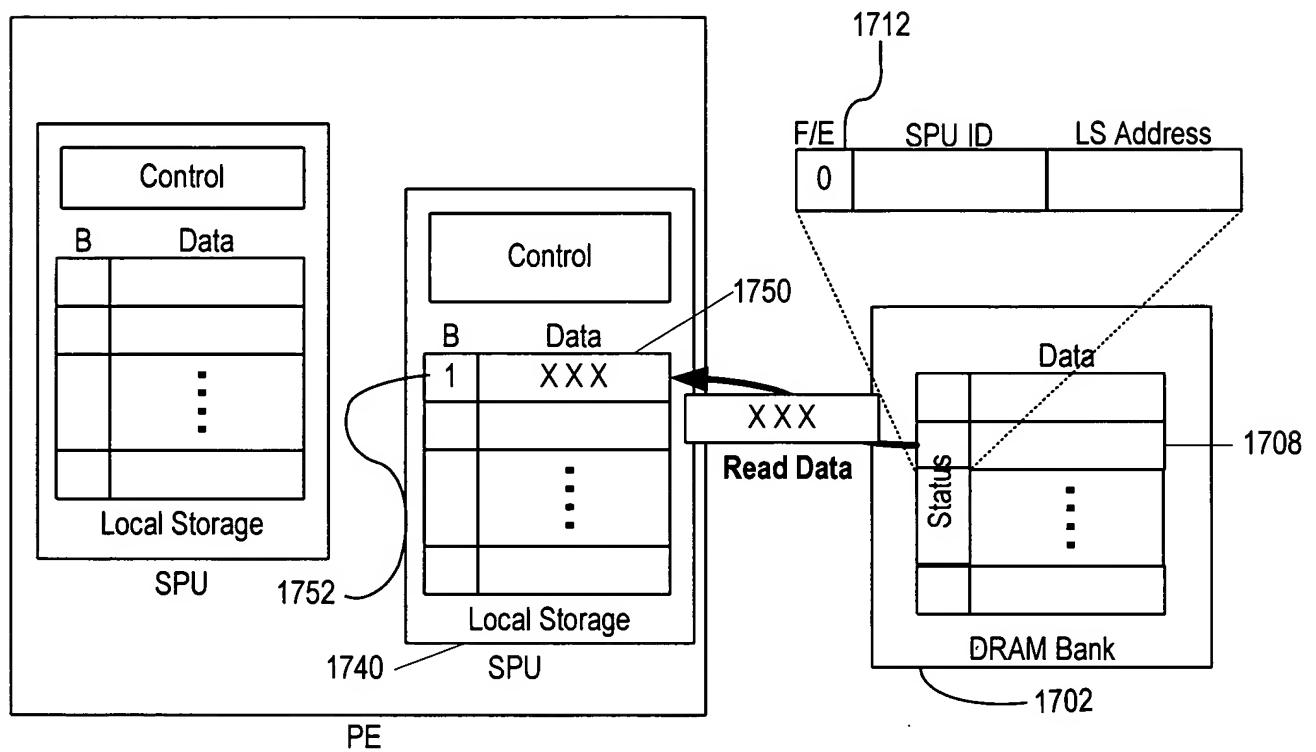


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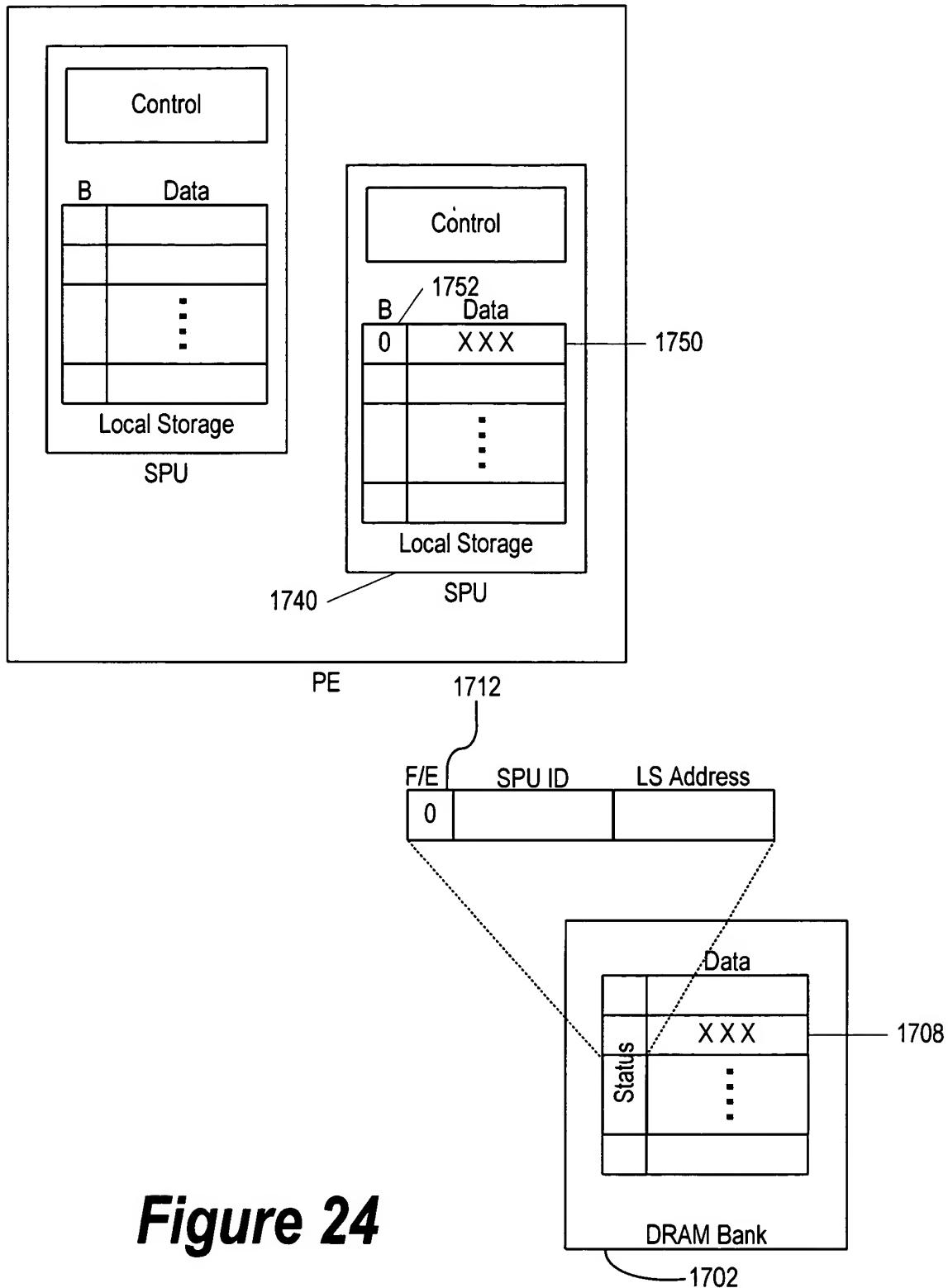


Figure 24

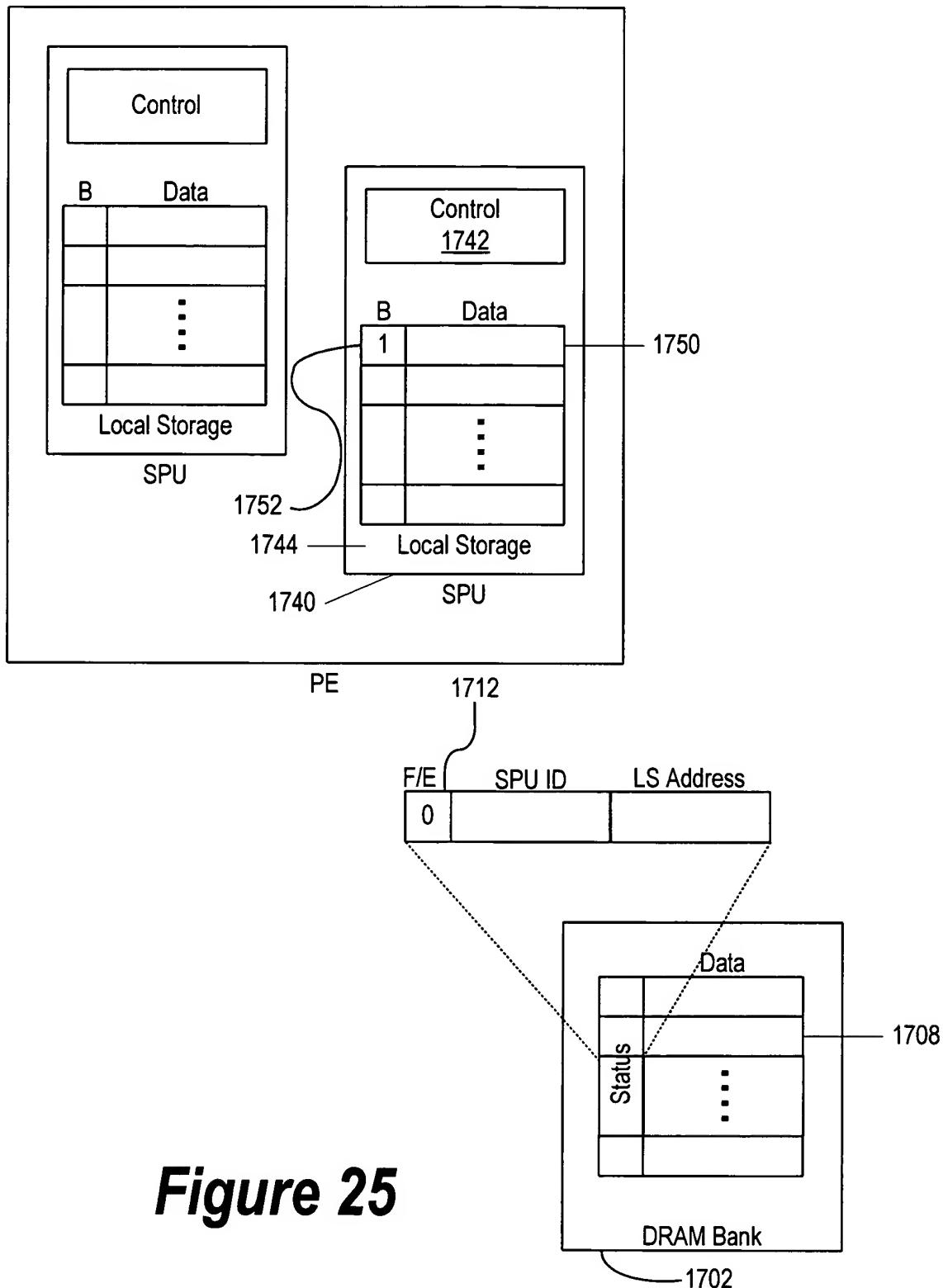


Figure 25

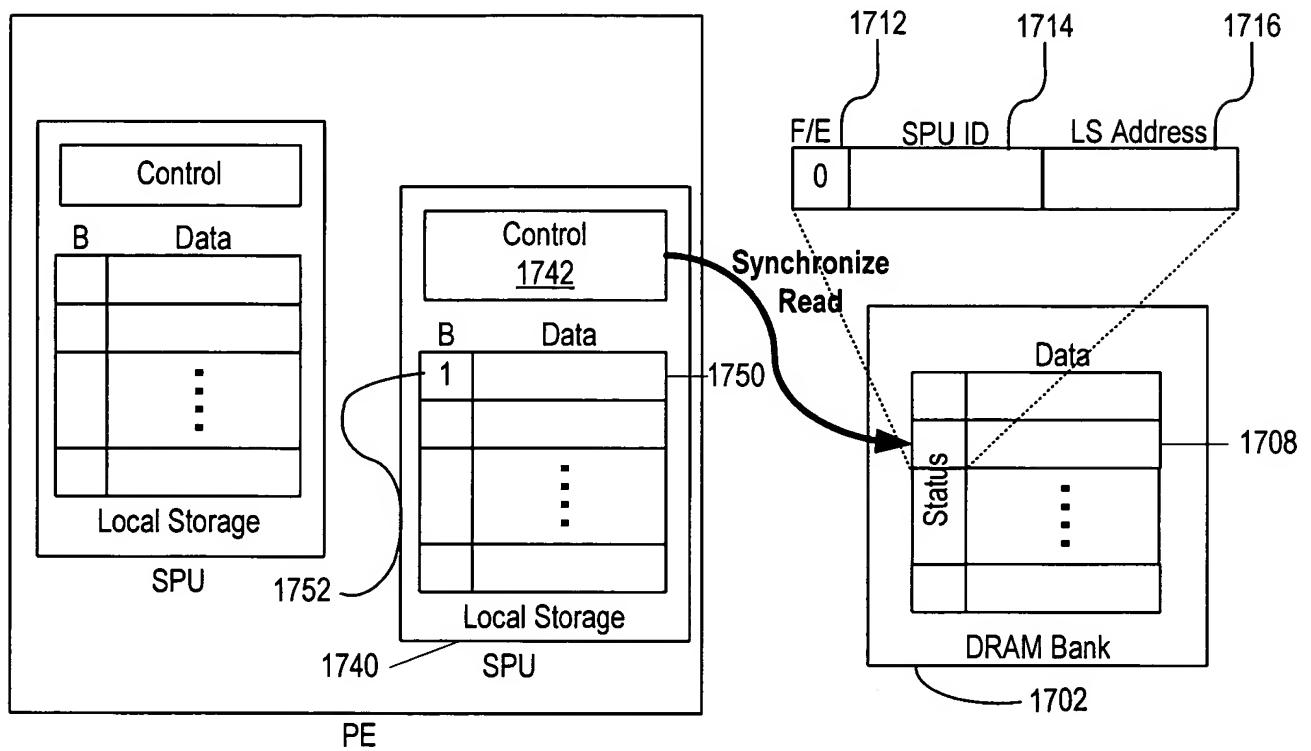


Figure 26

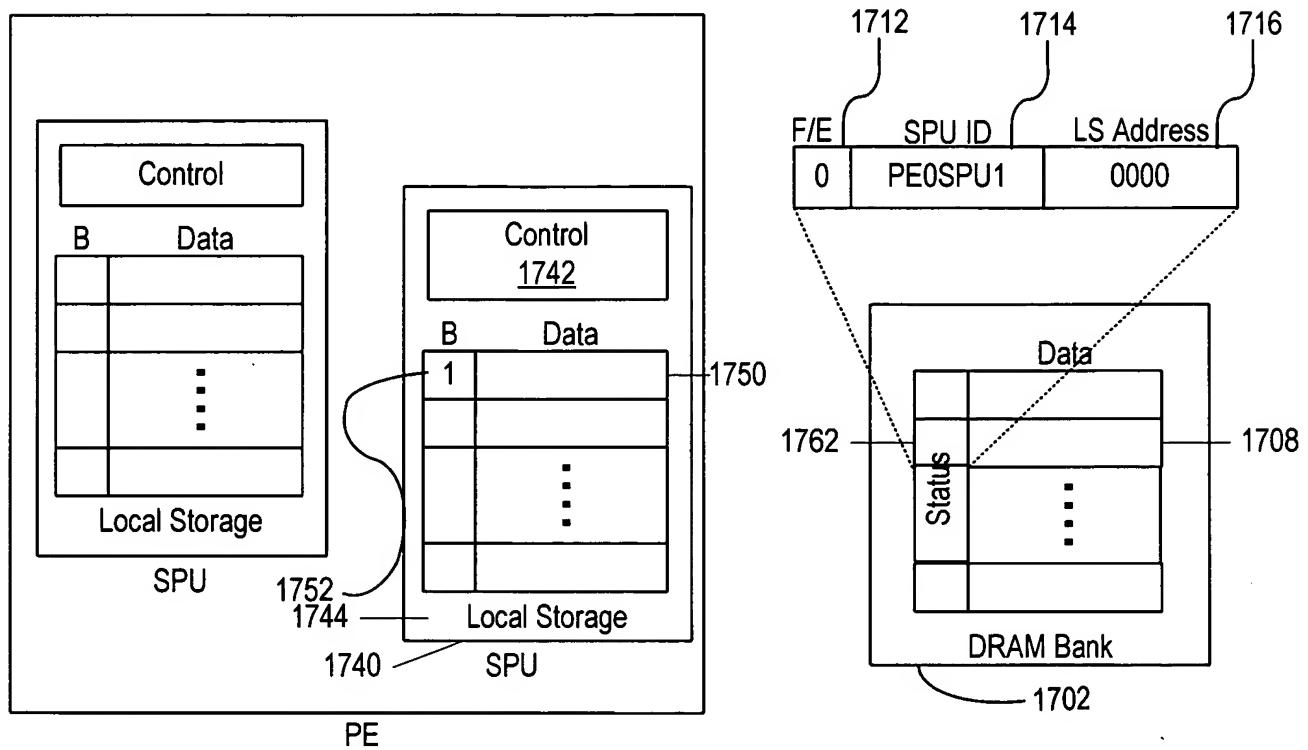


Figure 27

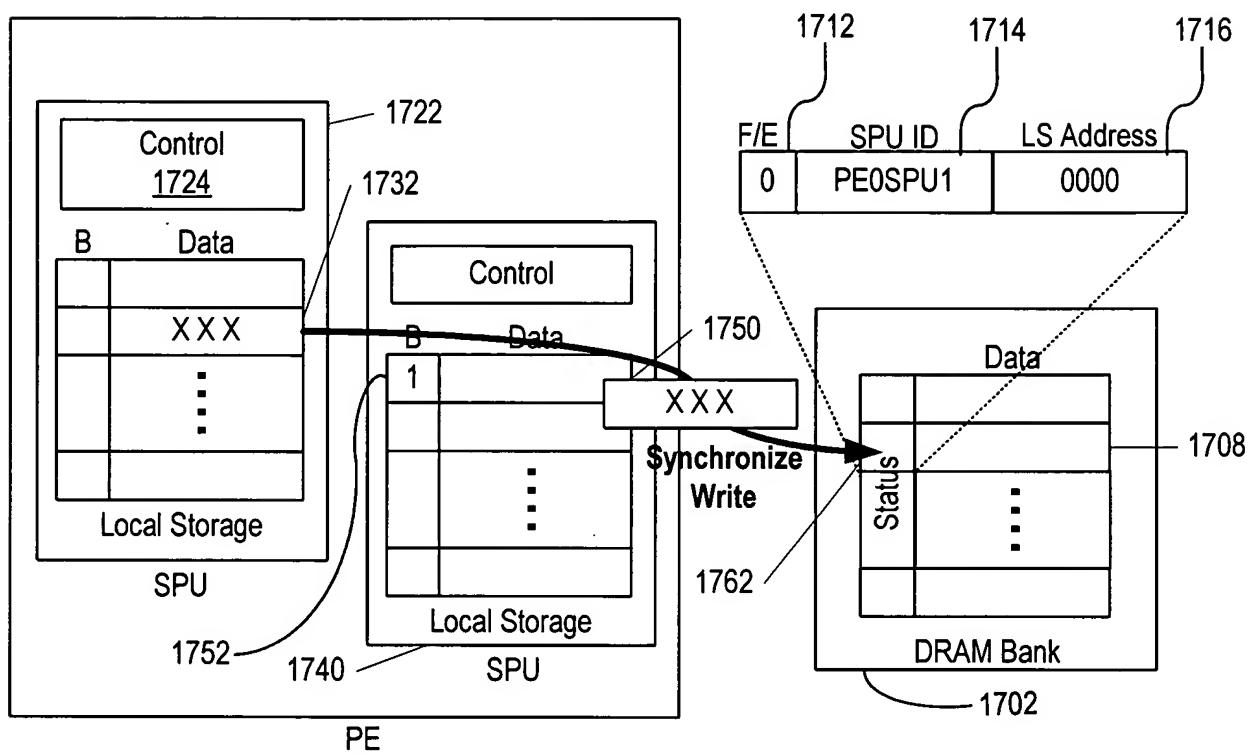


Figure 28

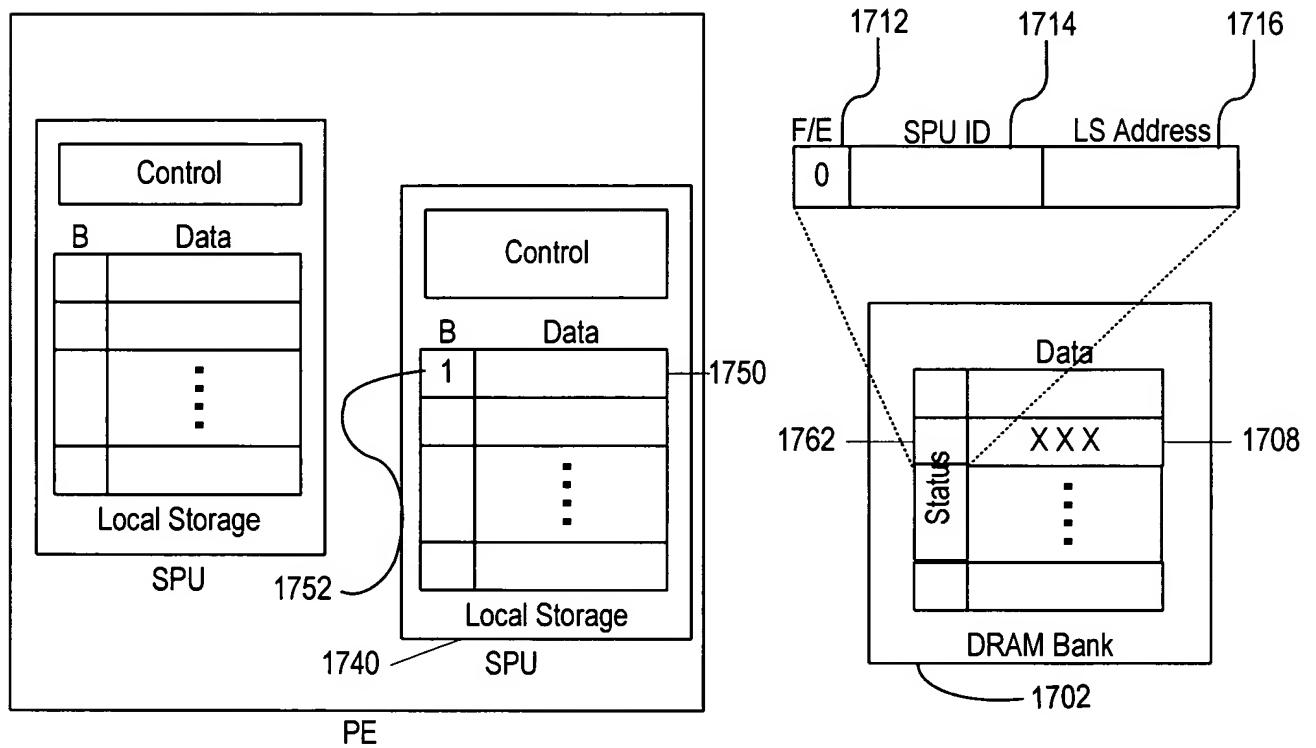


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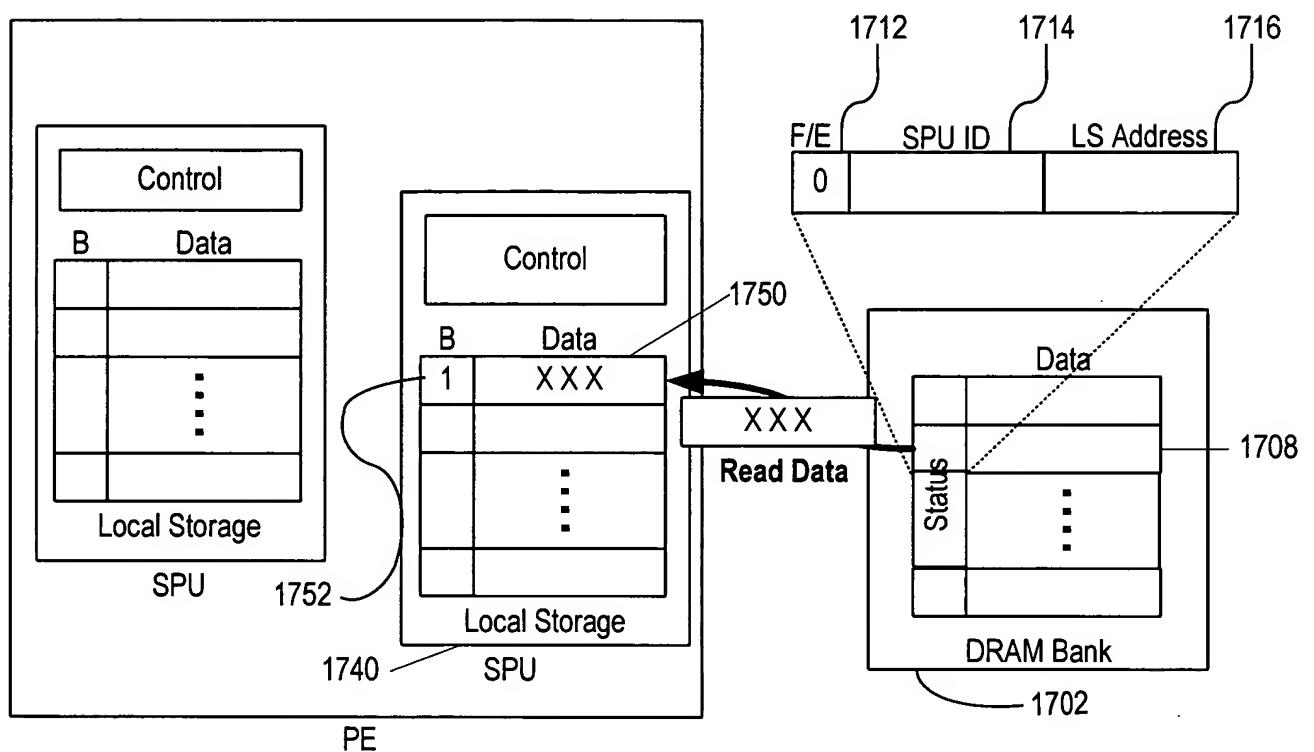


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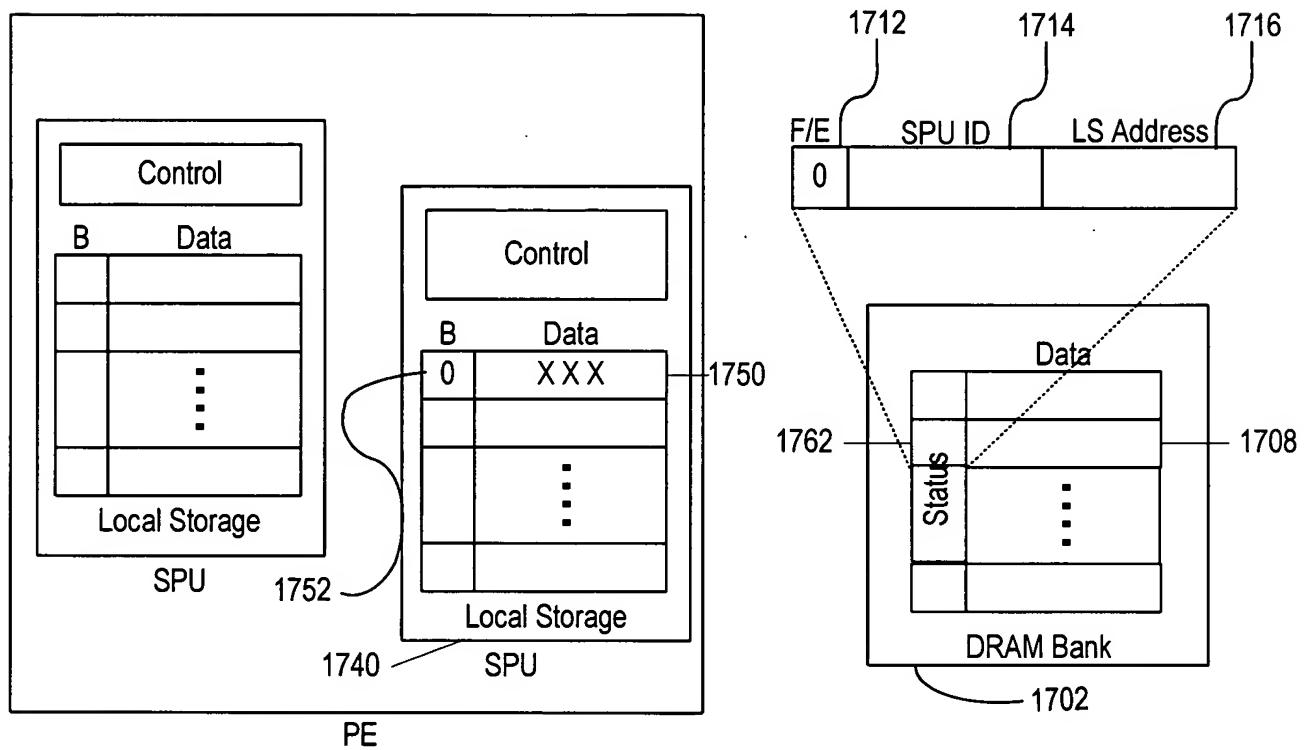


Figure 31

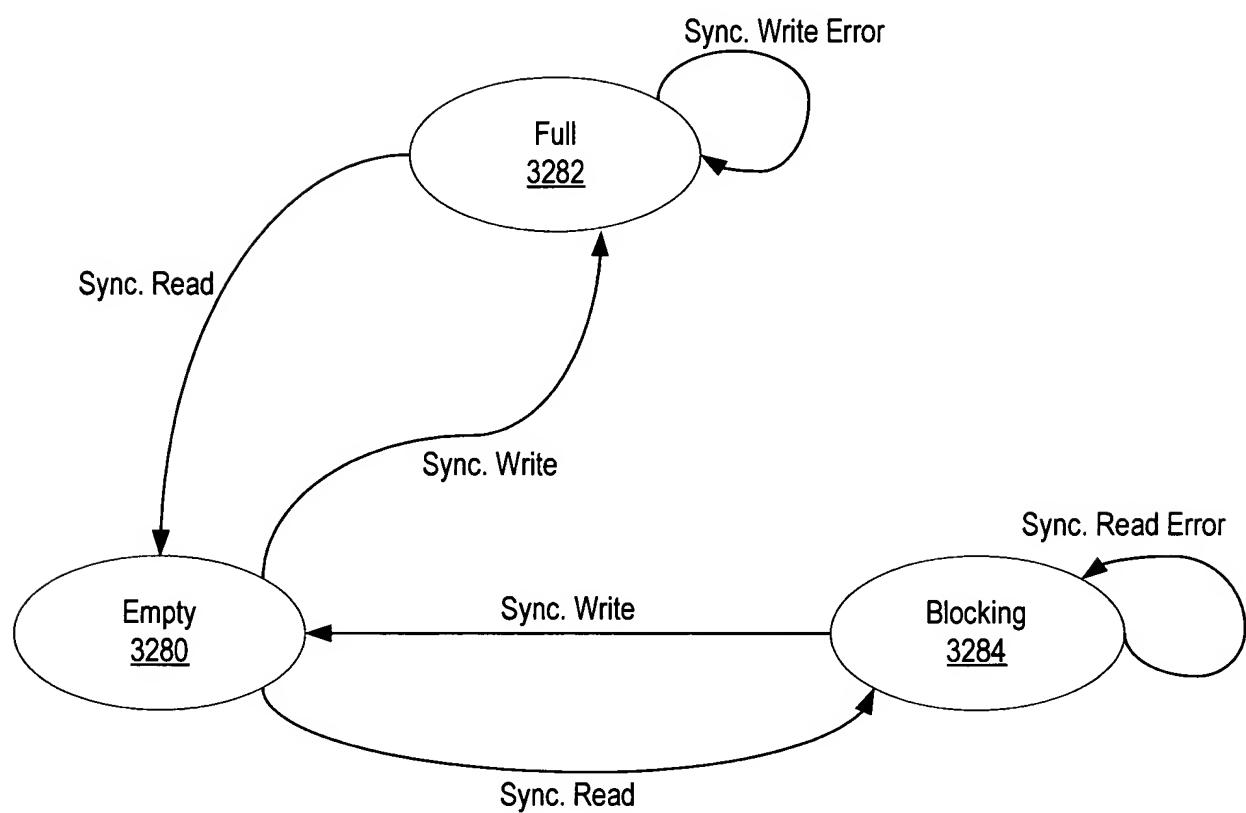


Figure 32

Key Control Table

ID	SPU Key	Key Mask
0	SPU Key	Key Mask
1	SPU Key	Key Mask
2	SPU Key	Key Mask
⋮		
7	SPU Key	Key Mask

Figure 33

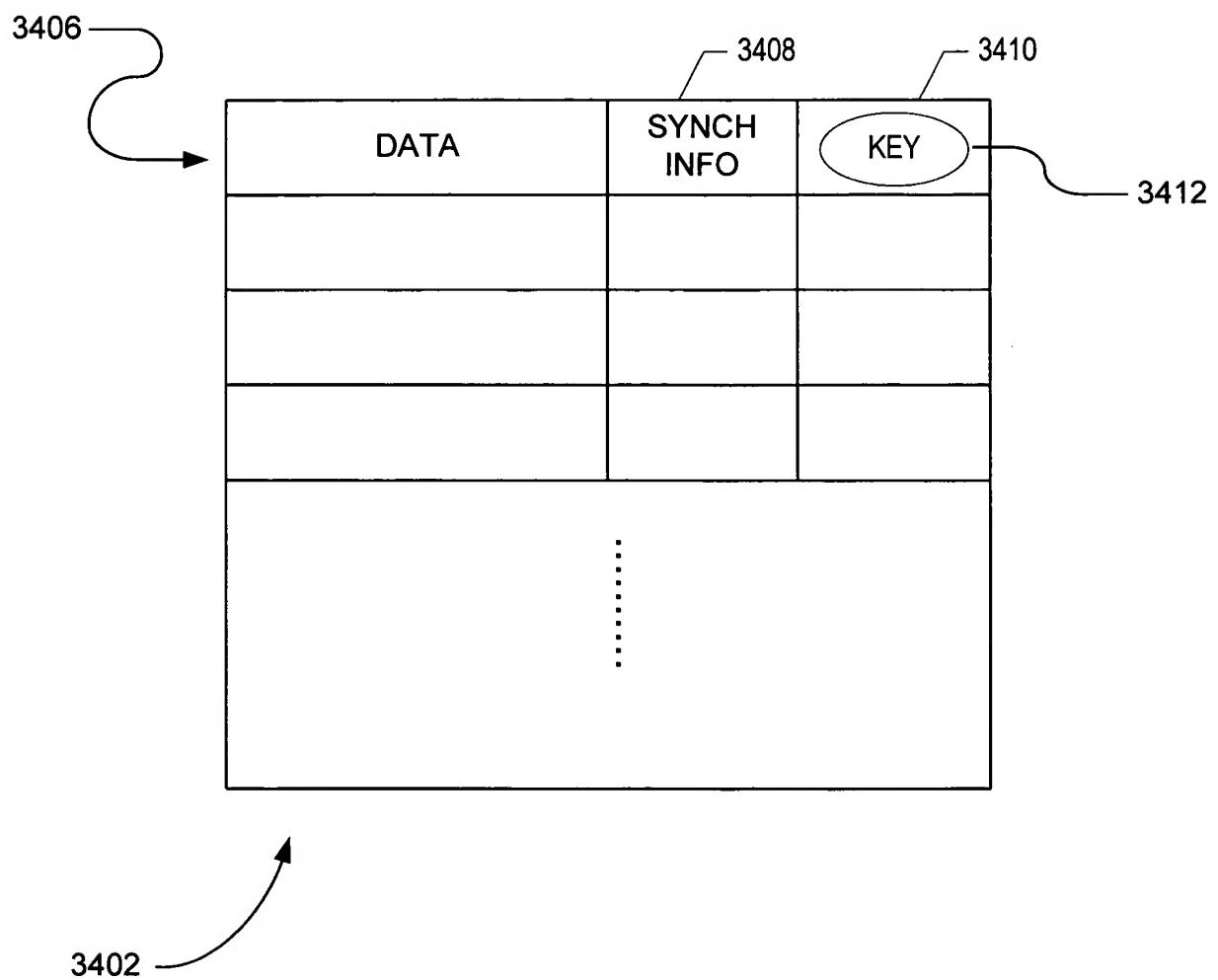


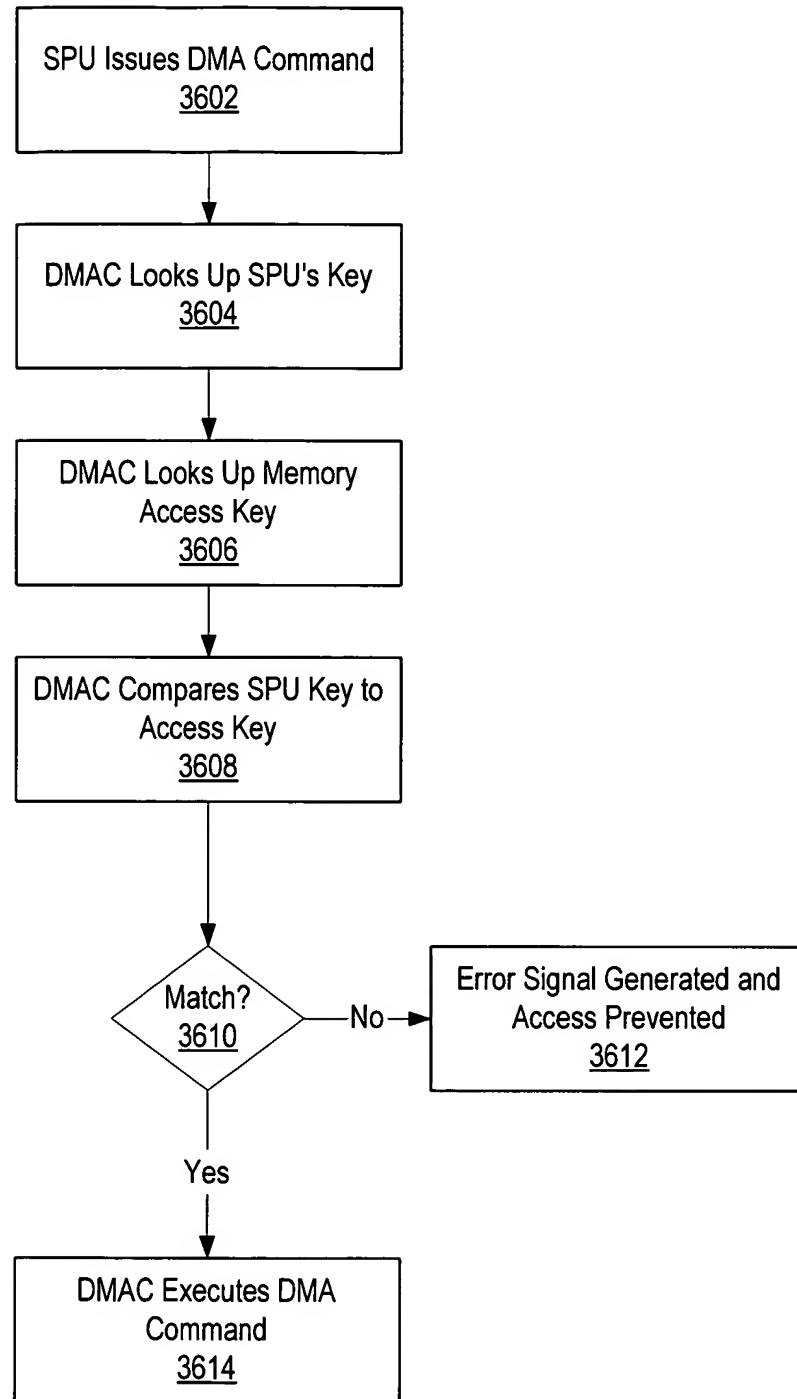
Figure 34

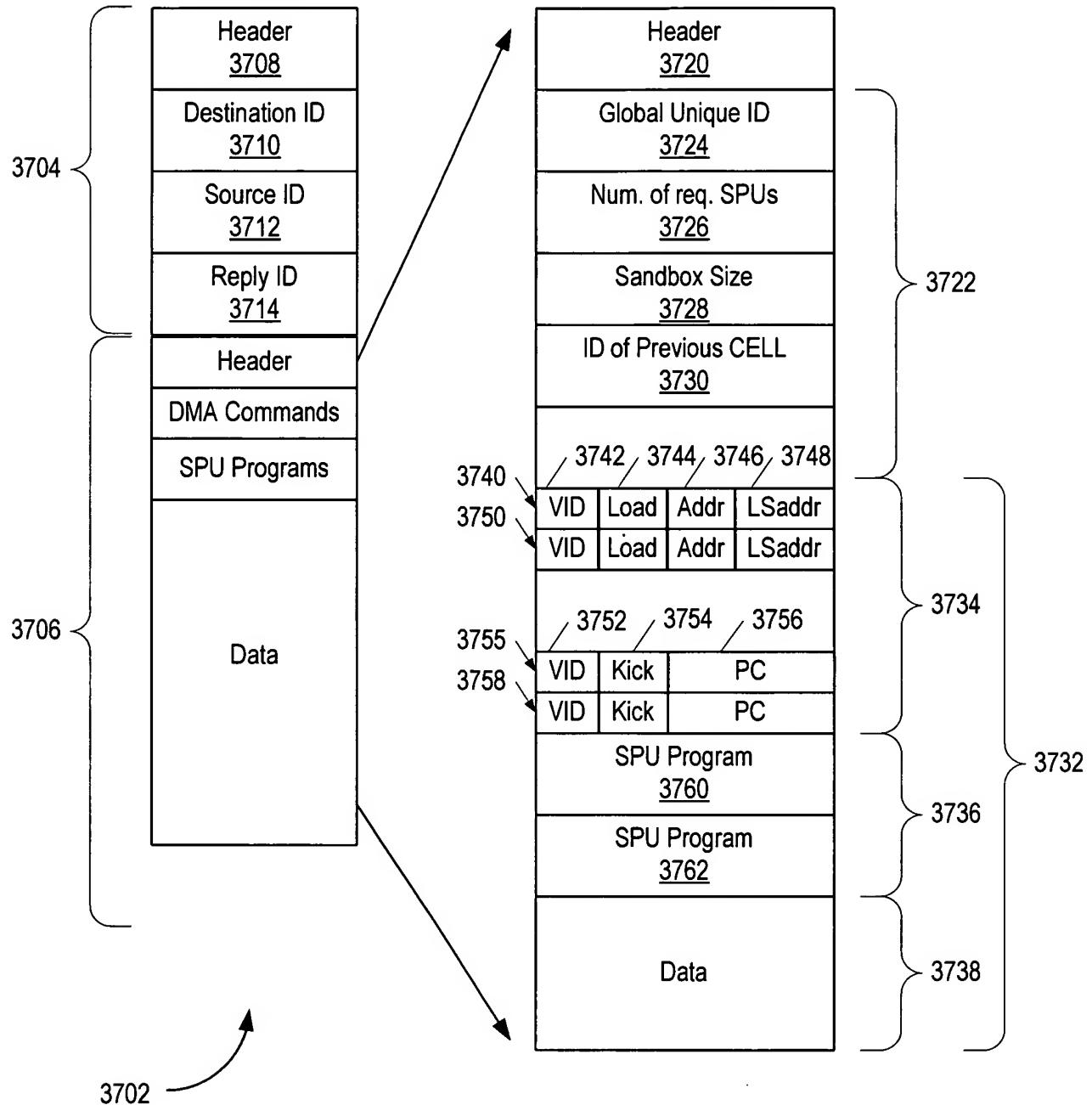
Memory Access Control Table

ID	3506	3508	3510	3512
0	Base	Size	Access Key	Access Key Mask
1	Base	Size	Access Key	Access Key Mask
2	Base	Size	Access Key	Access Key Mask
63	Base	Size	Access Key	Access Key Mask

3502

Figure 35

**Figure 36**

**Figure 37**

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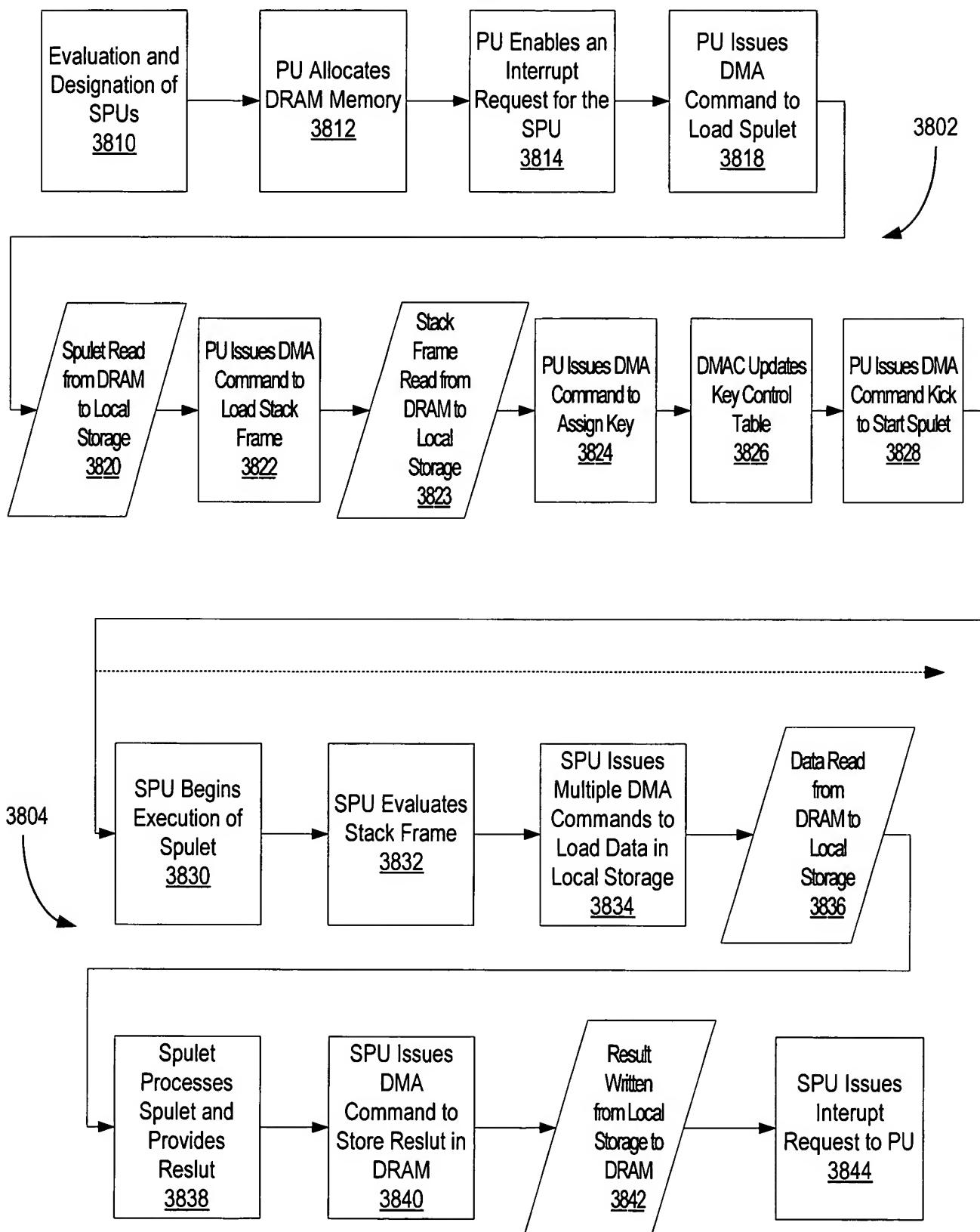


Figure 38

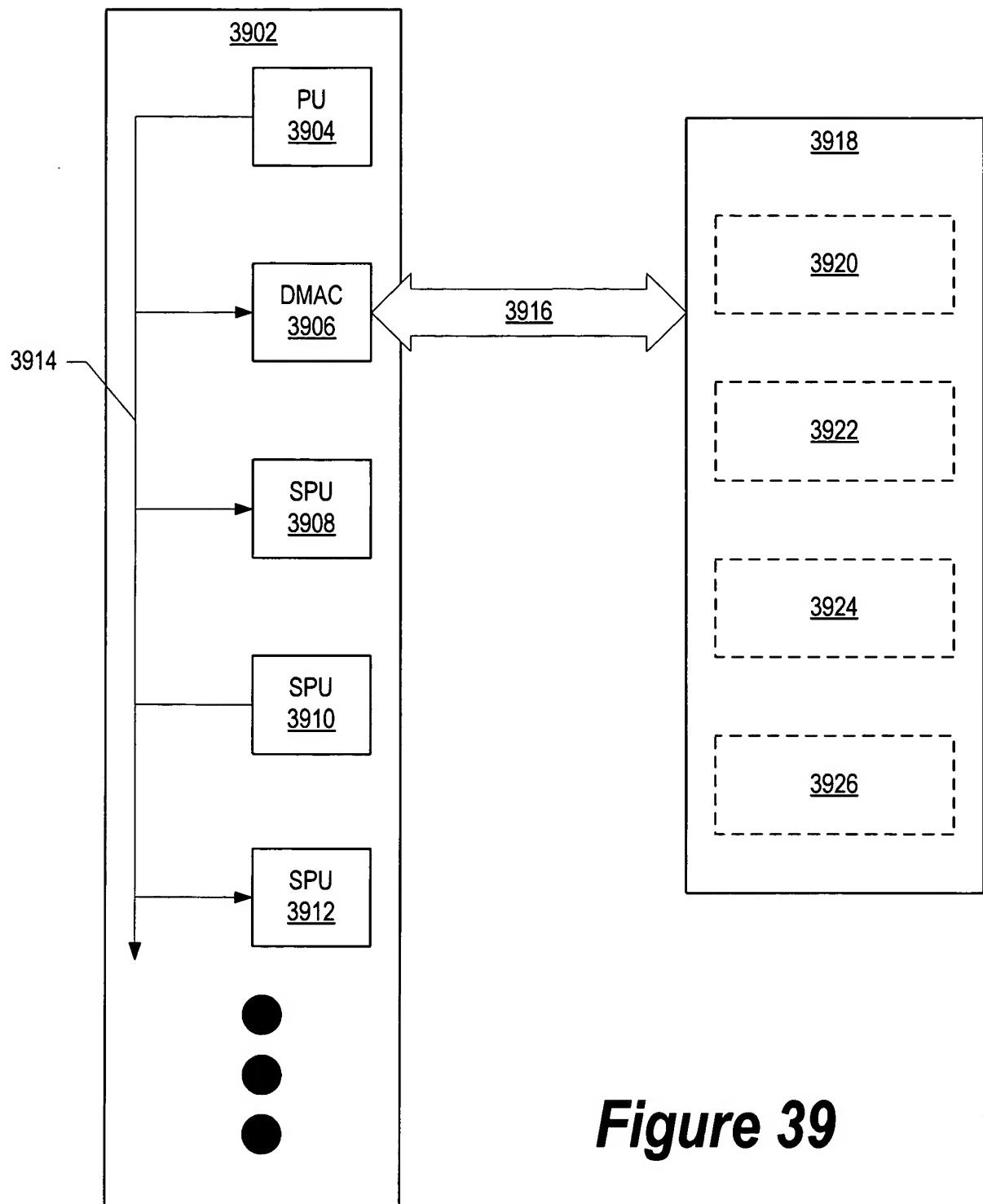
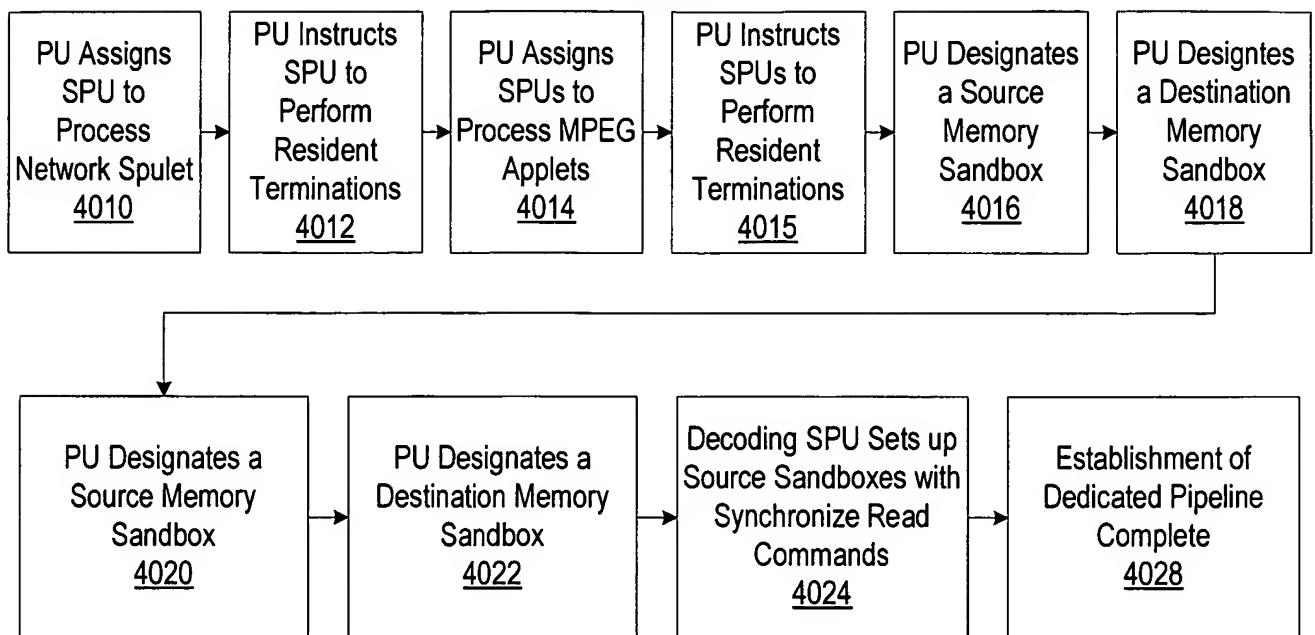
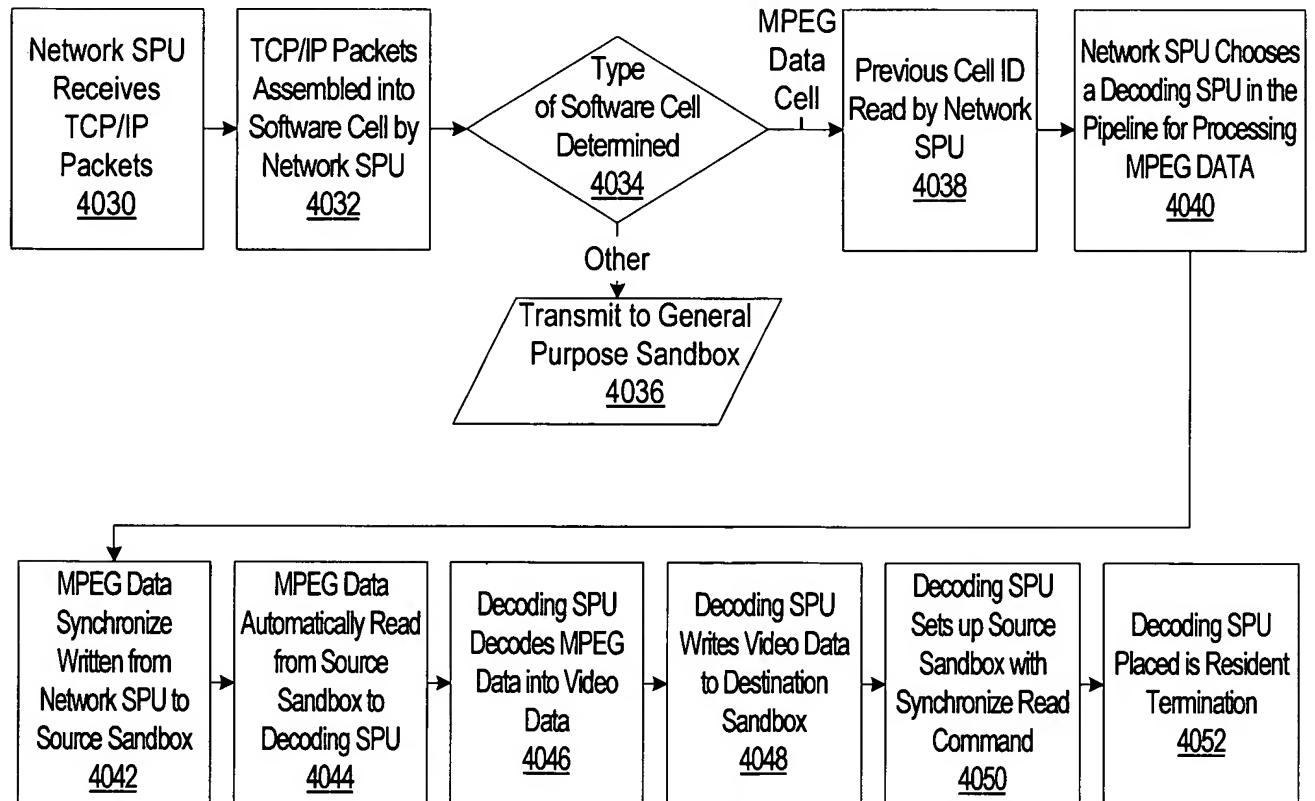


Figure 39

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**Figure 40A****Figure 40B**

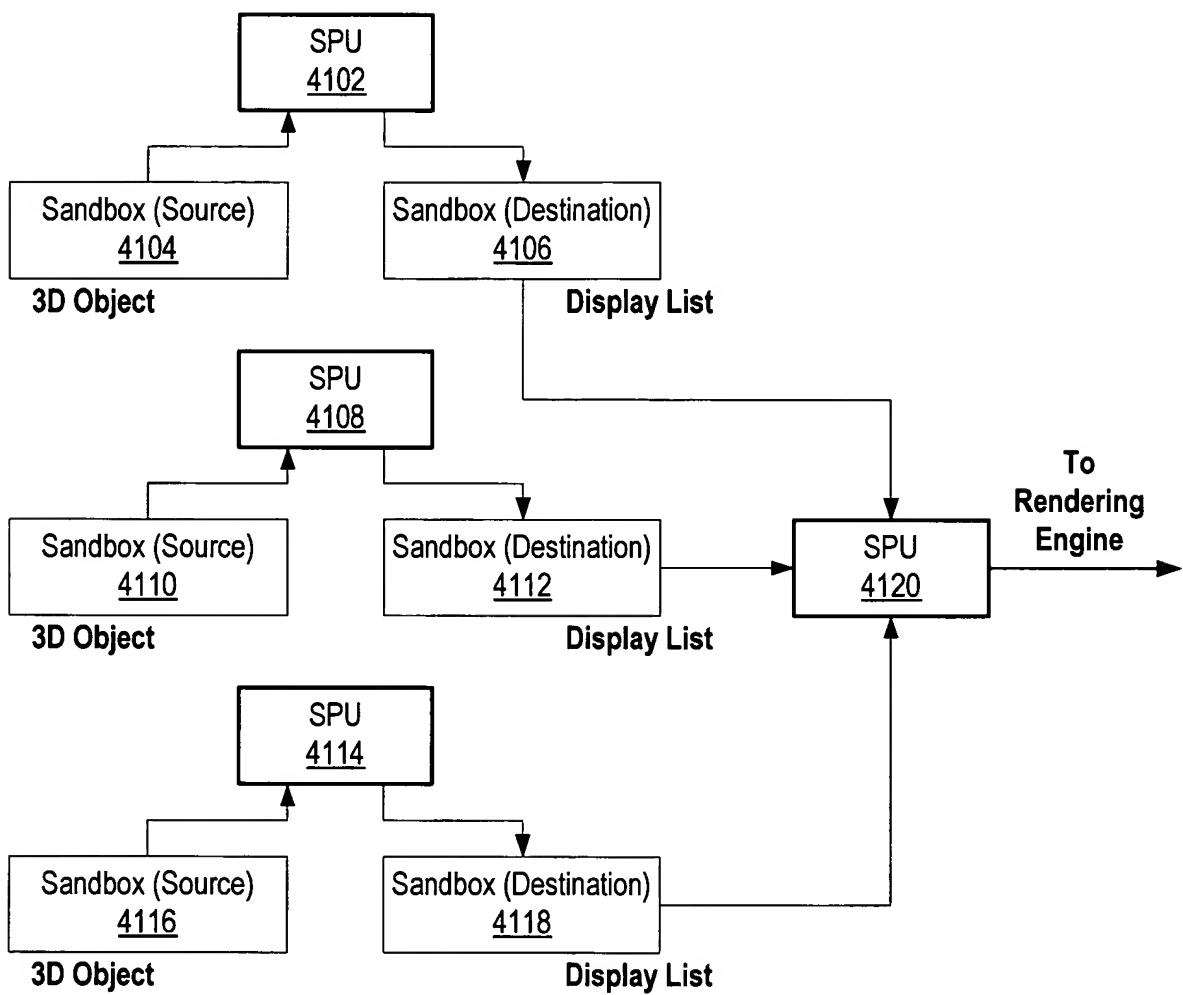


Figure 41

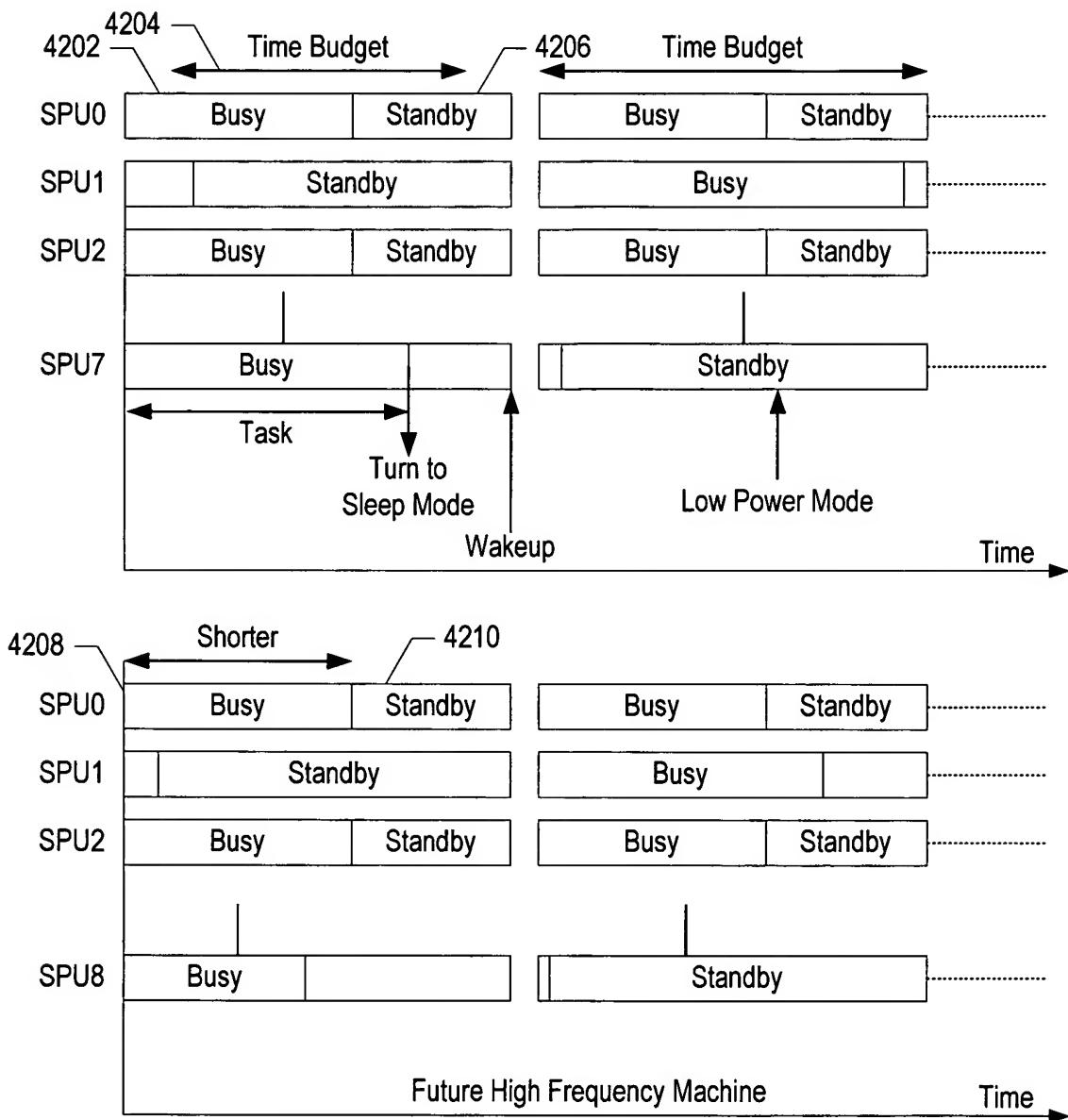


Figure 42

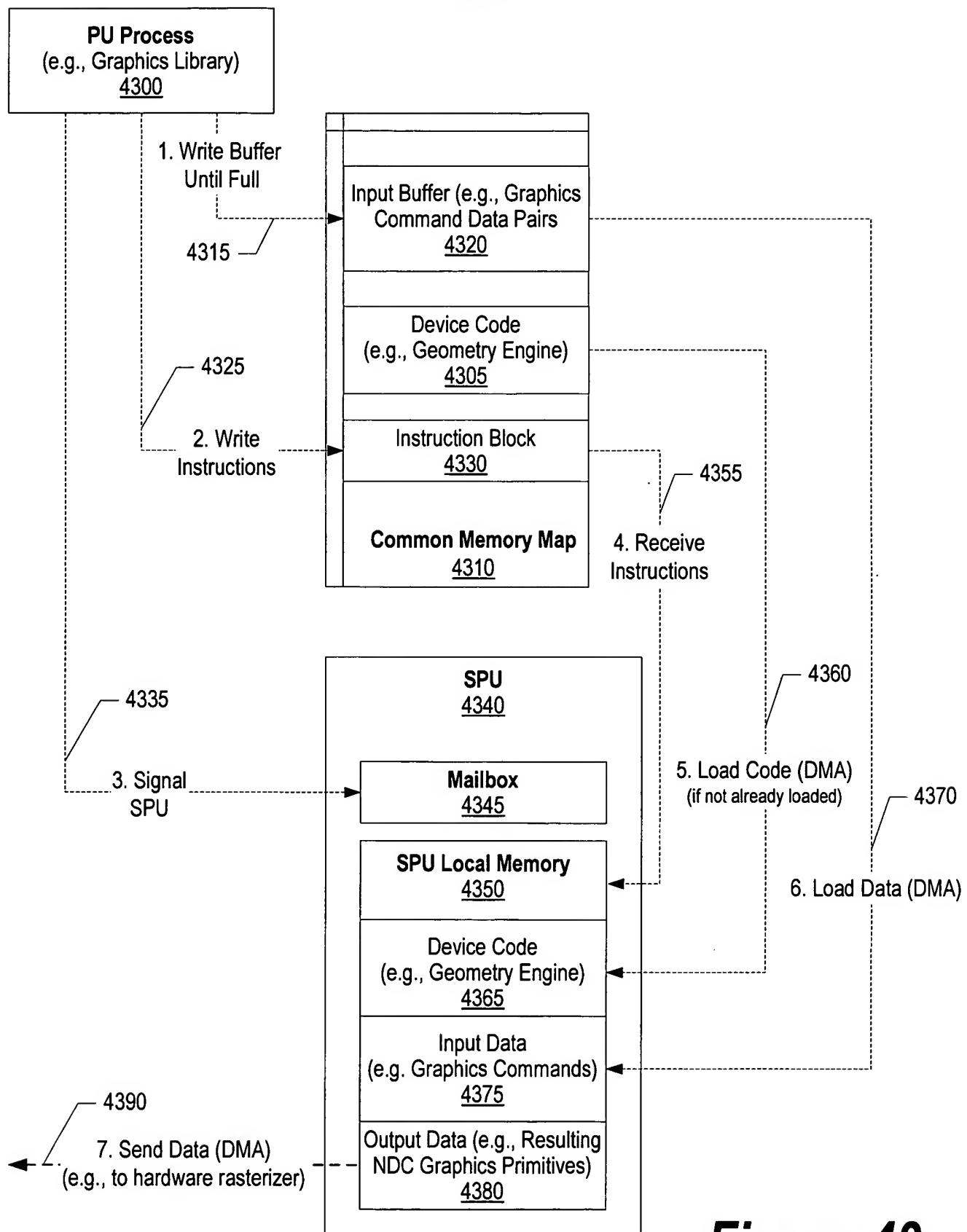


Figure 43

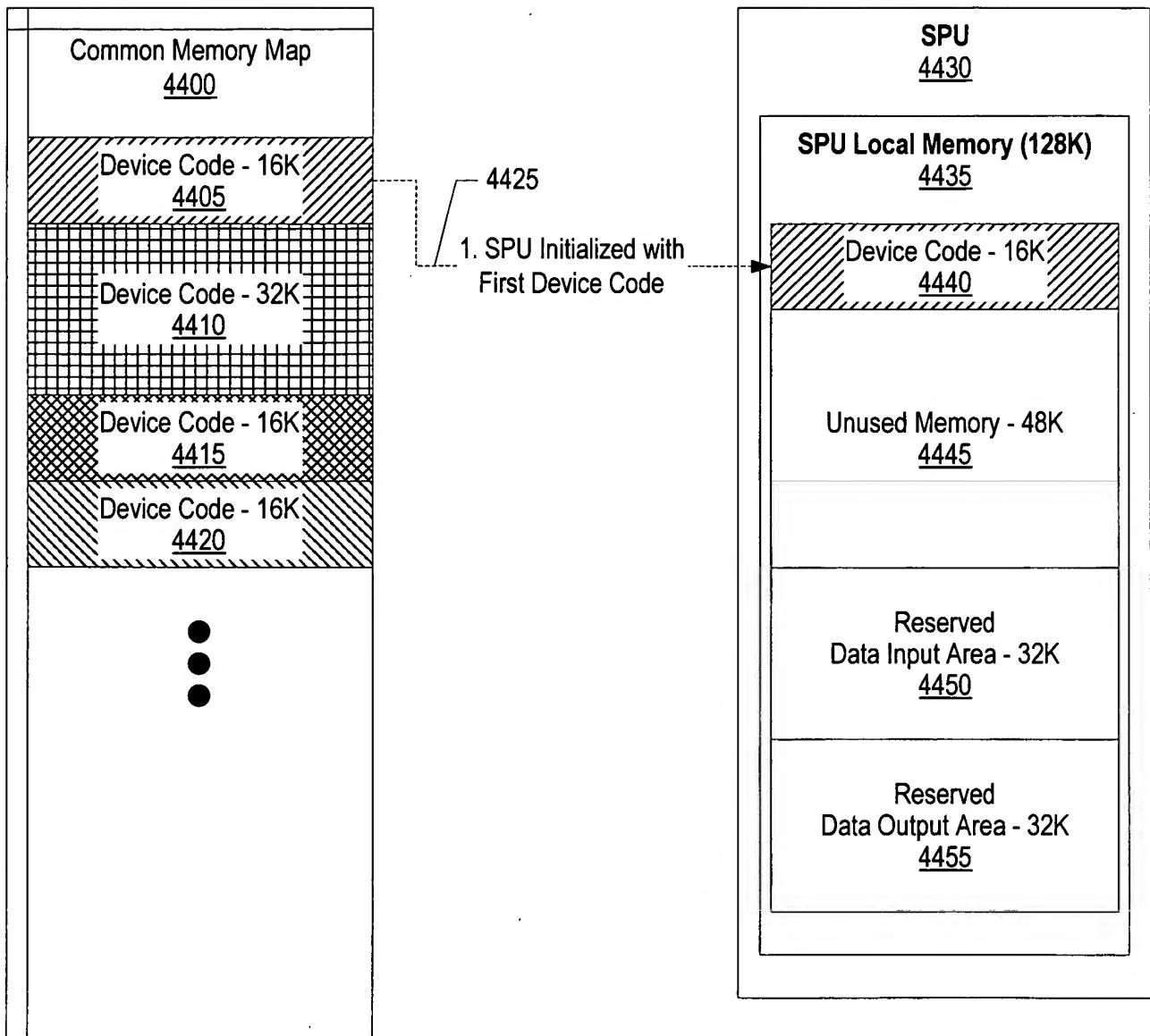


Figure 44

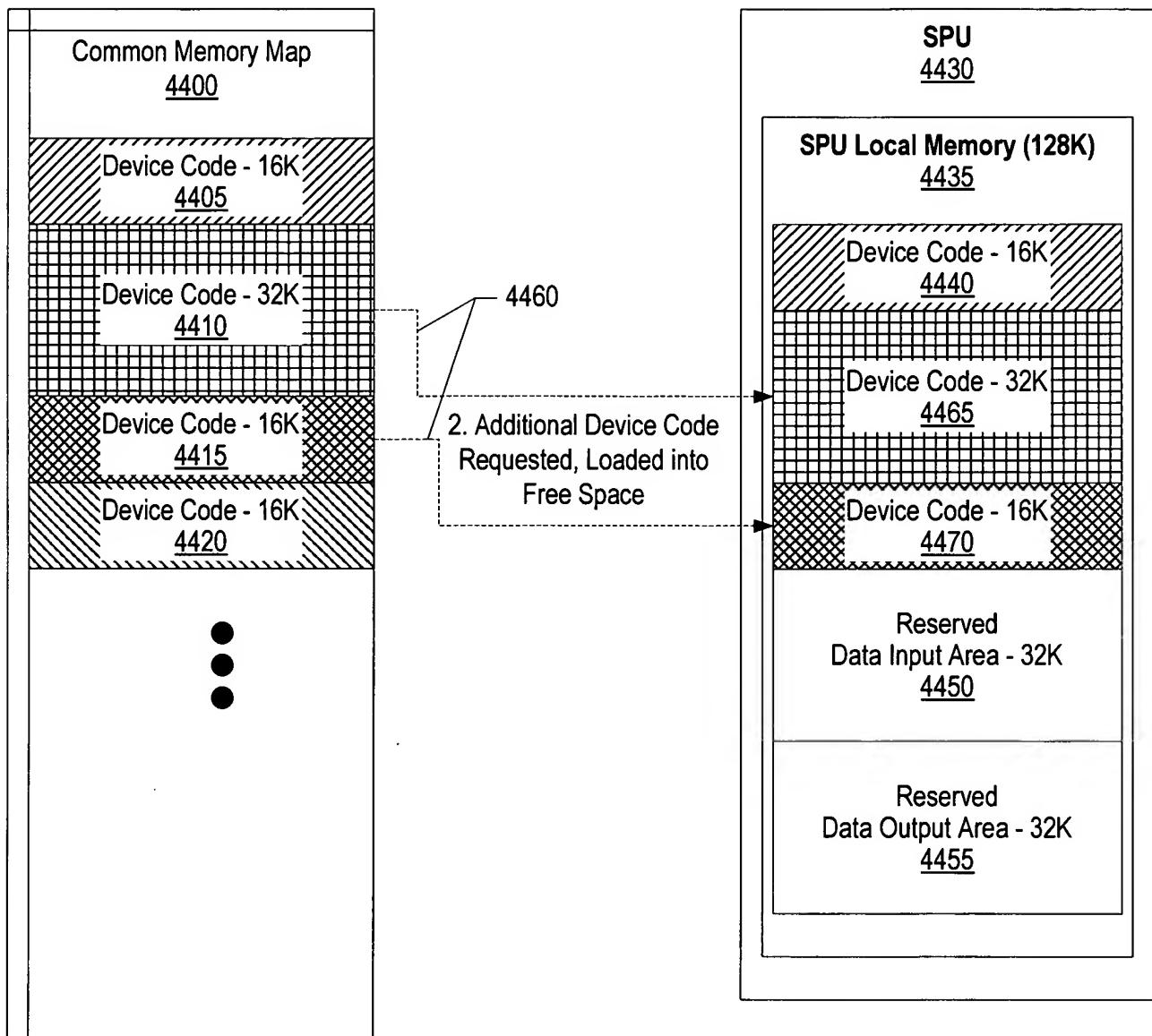


Figure 45

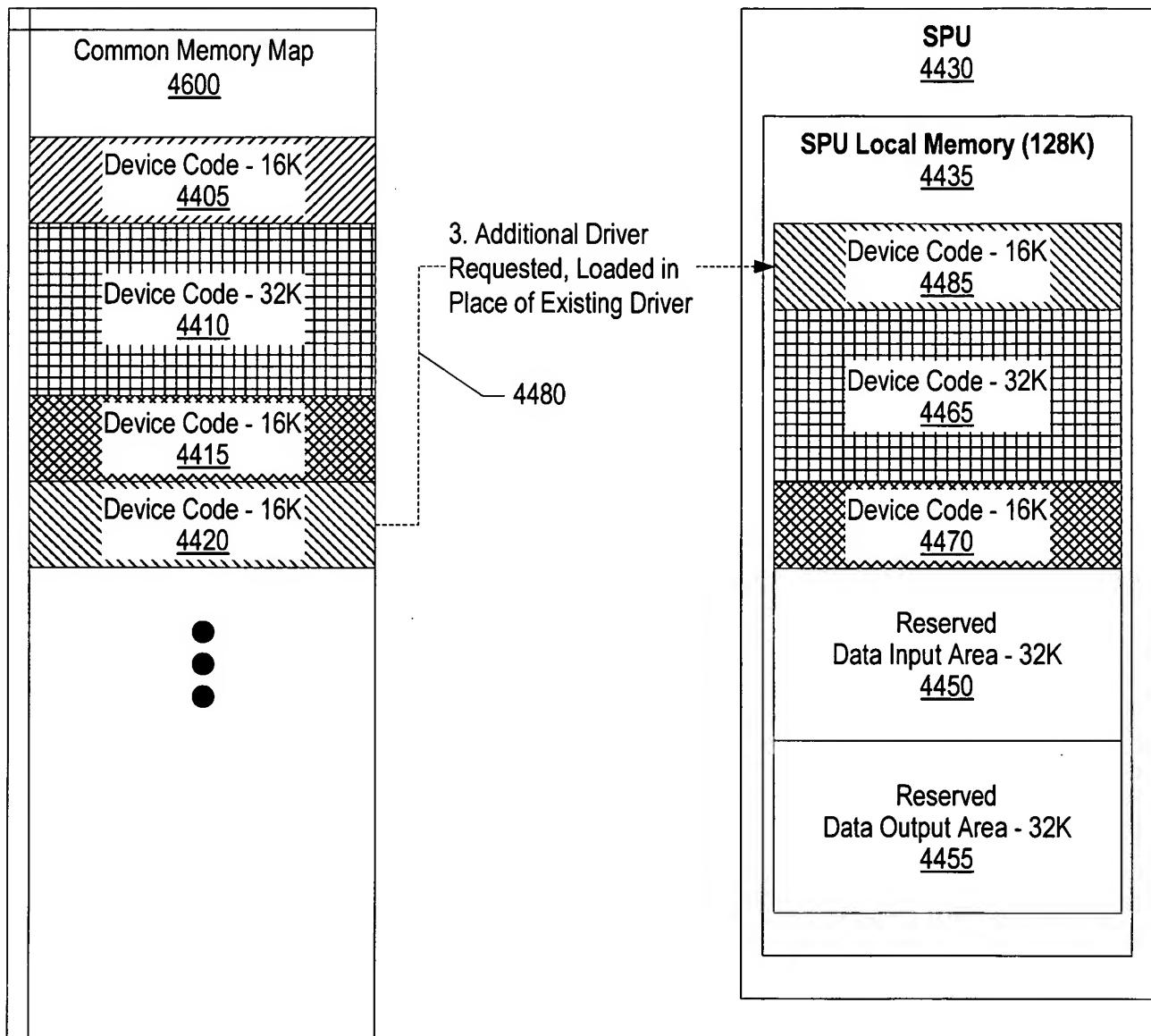


Figure 46

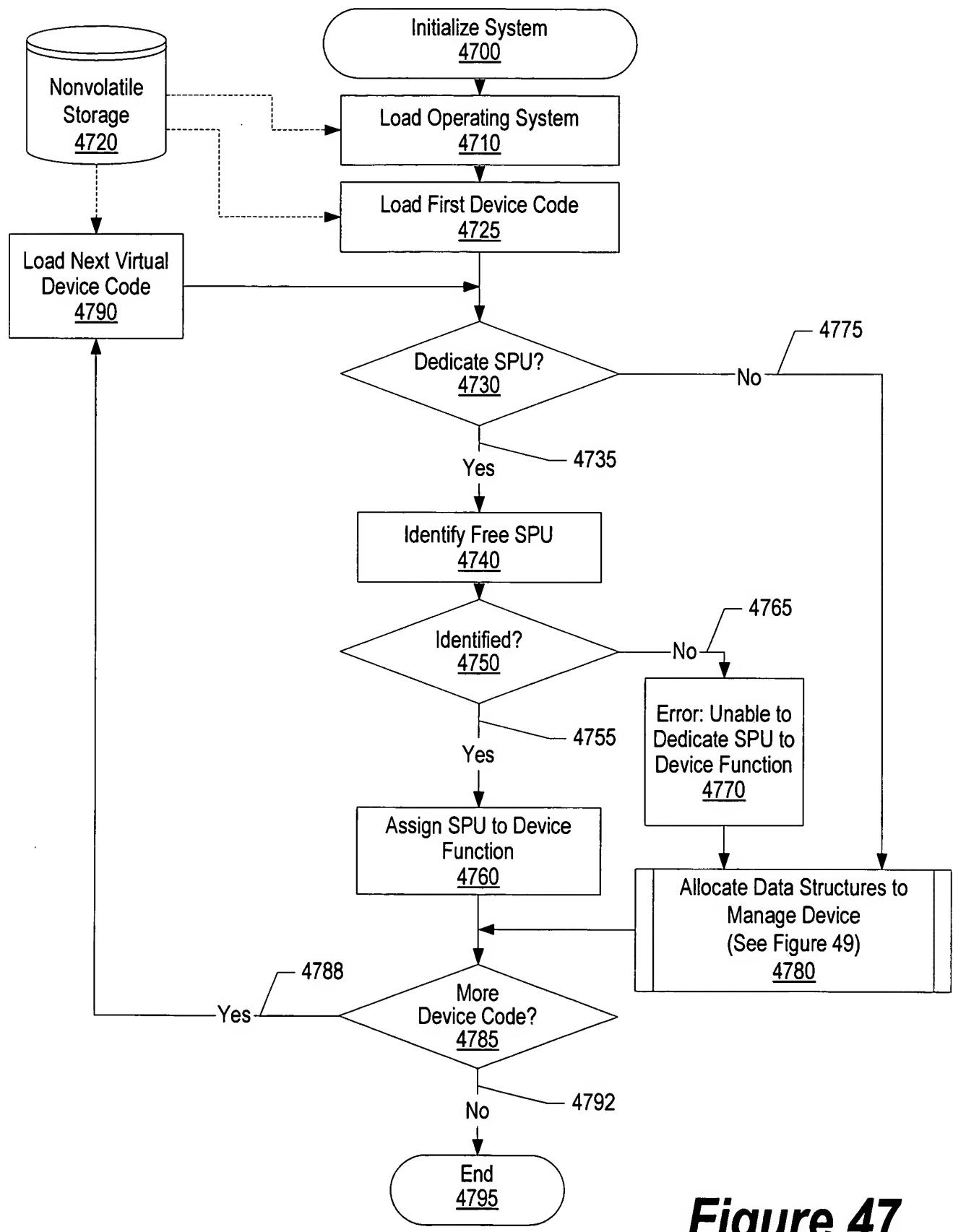


Figure 47

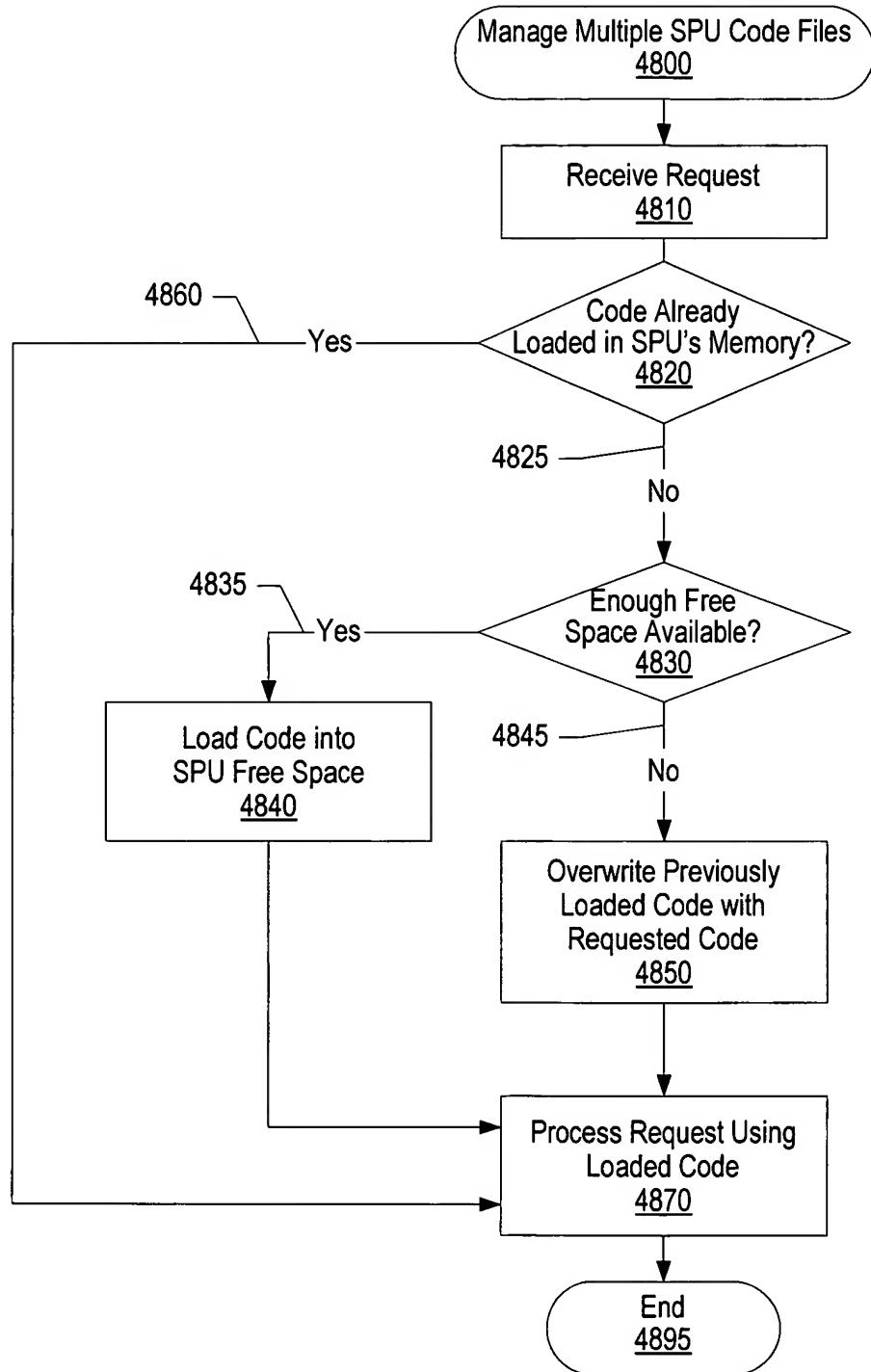


Figure 48

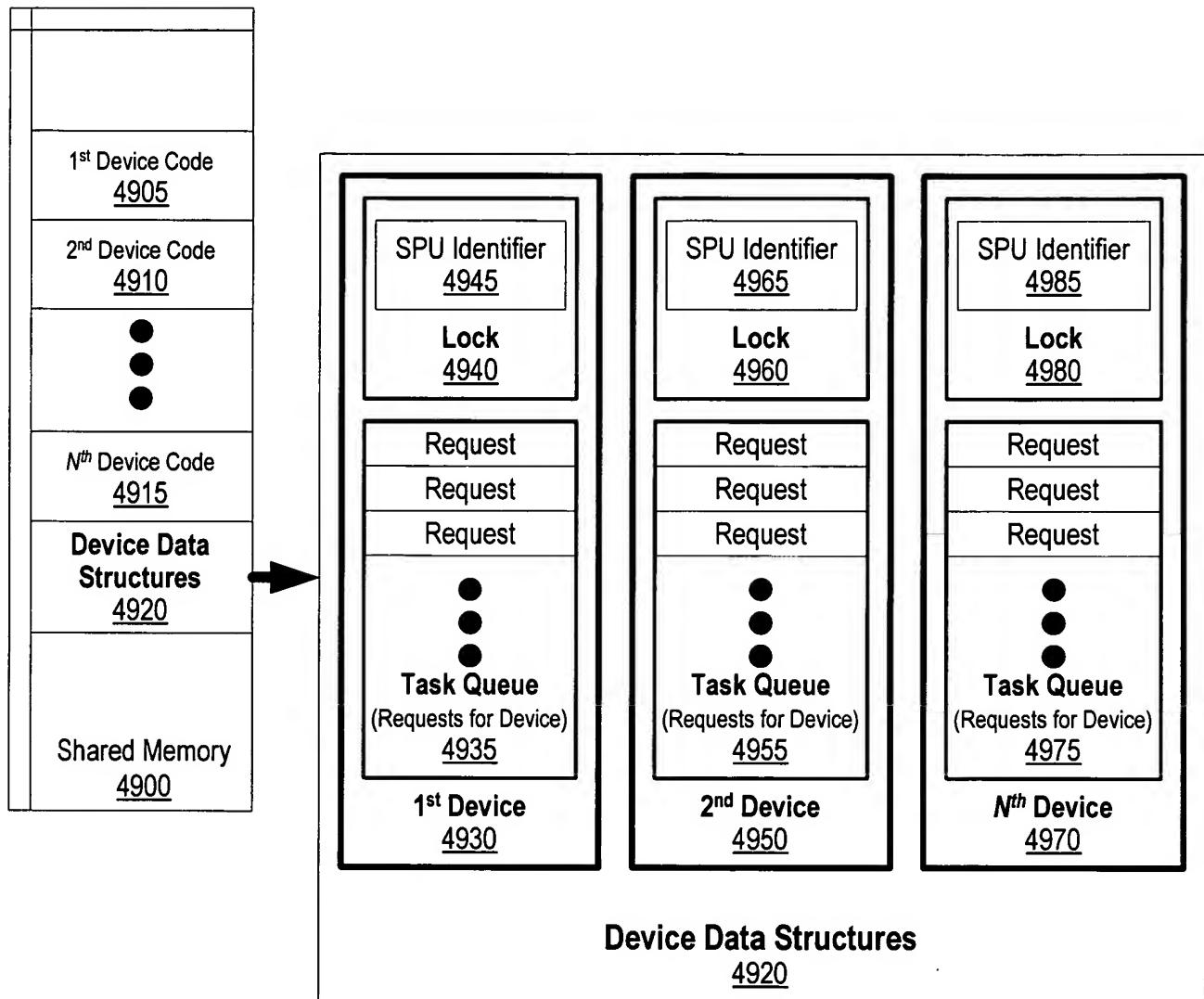


Figure 49

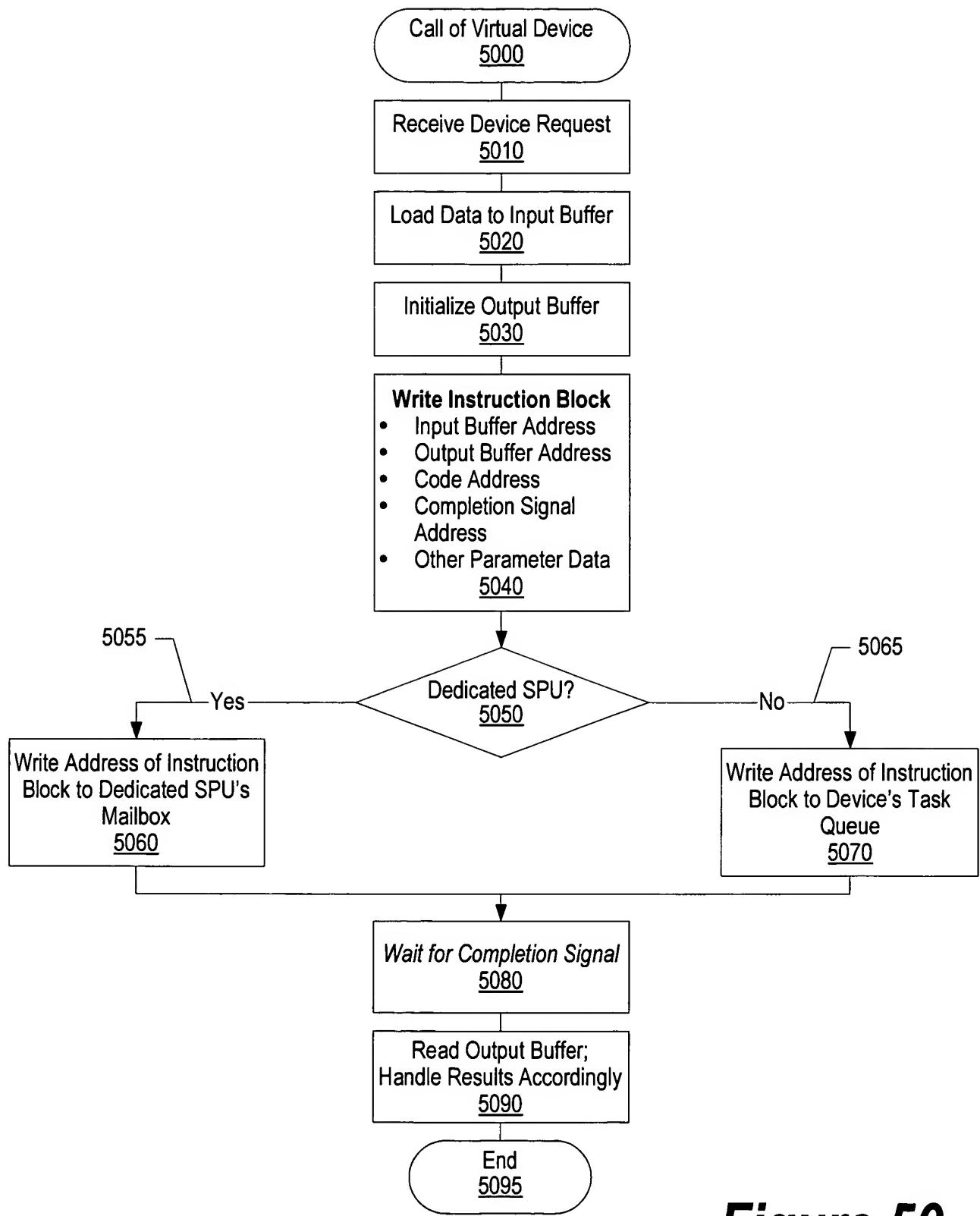


Figure 50

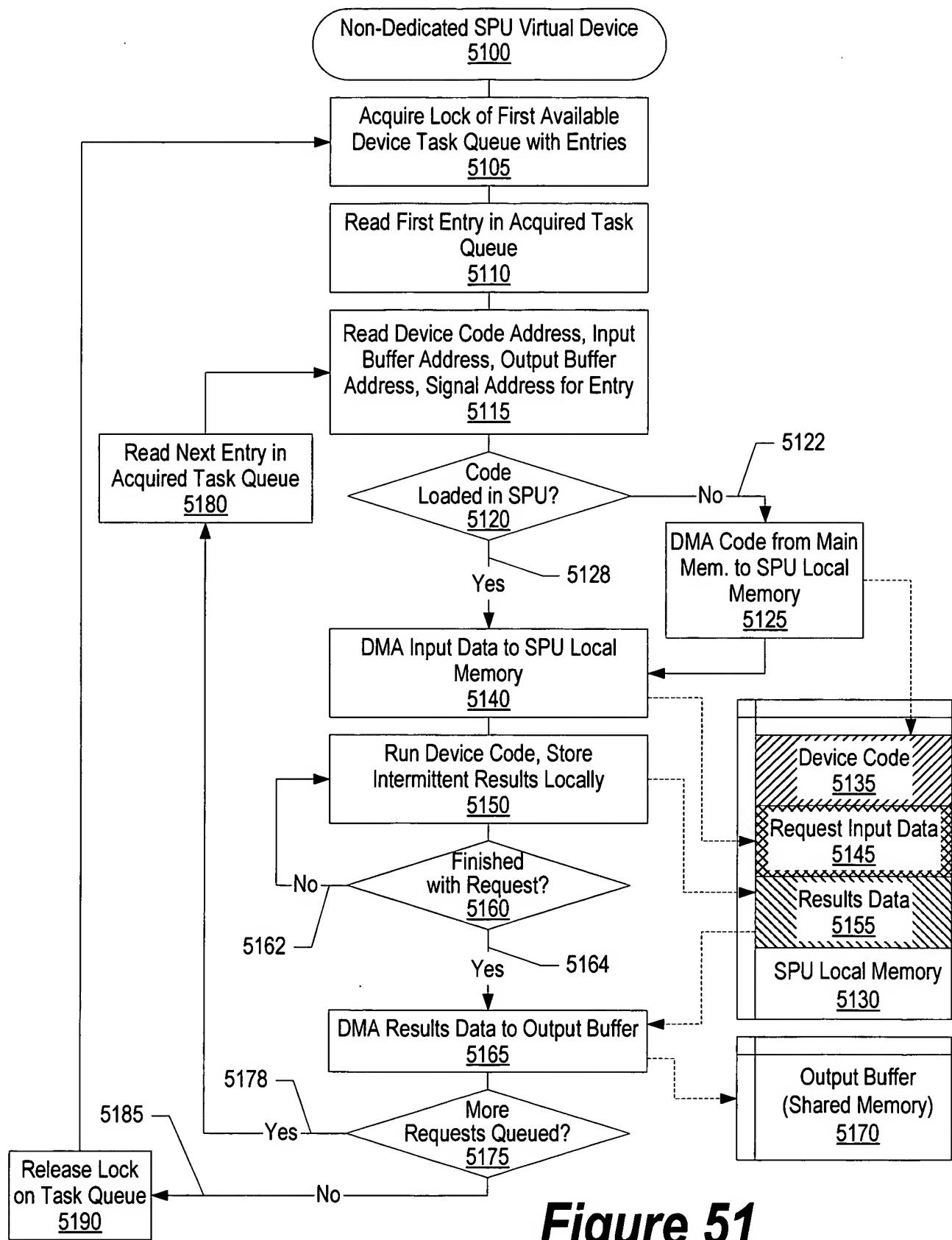


Figure 51

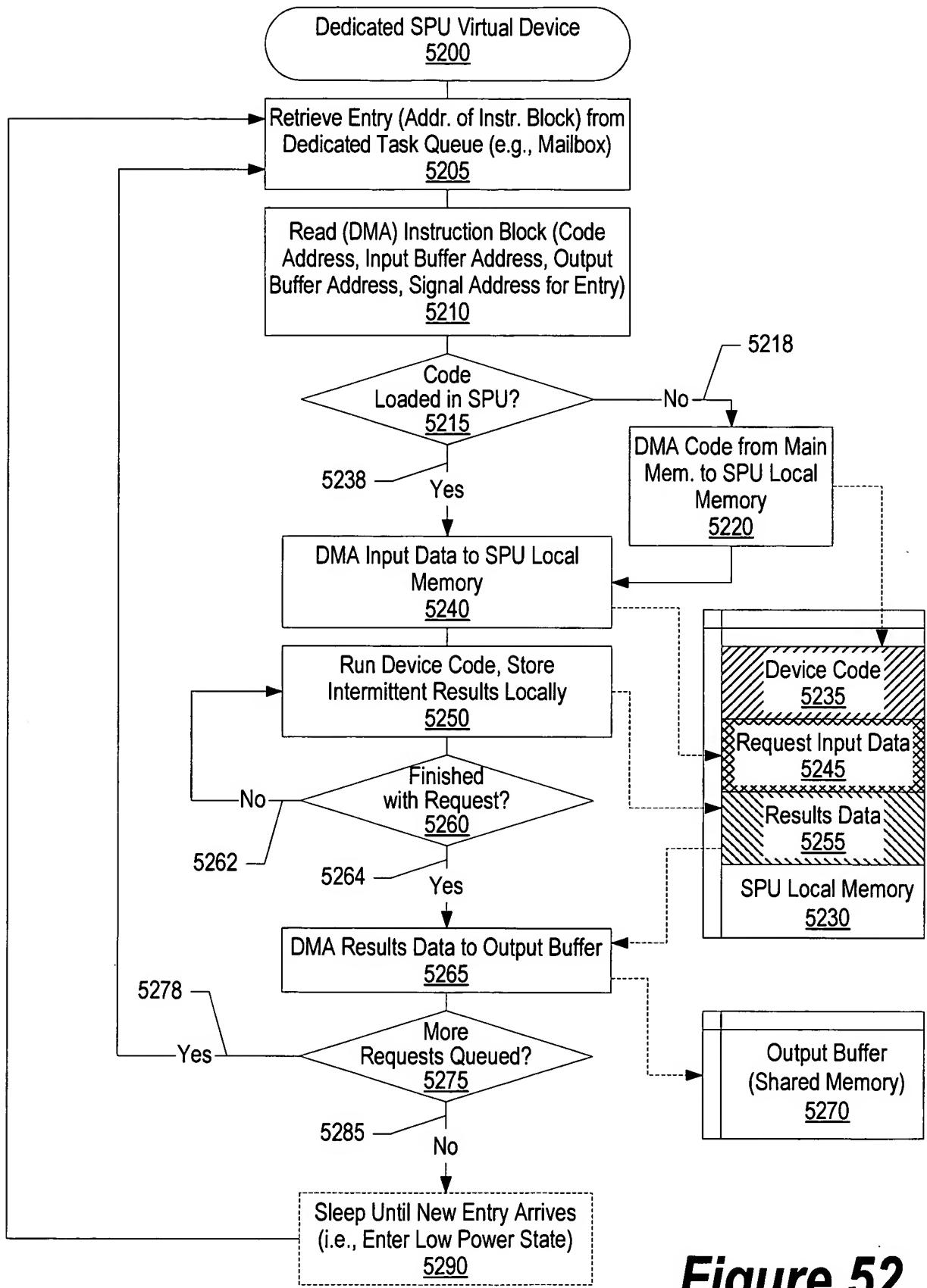
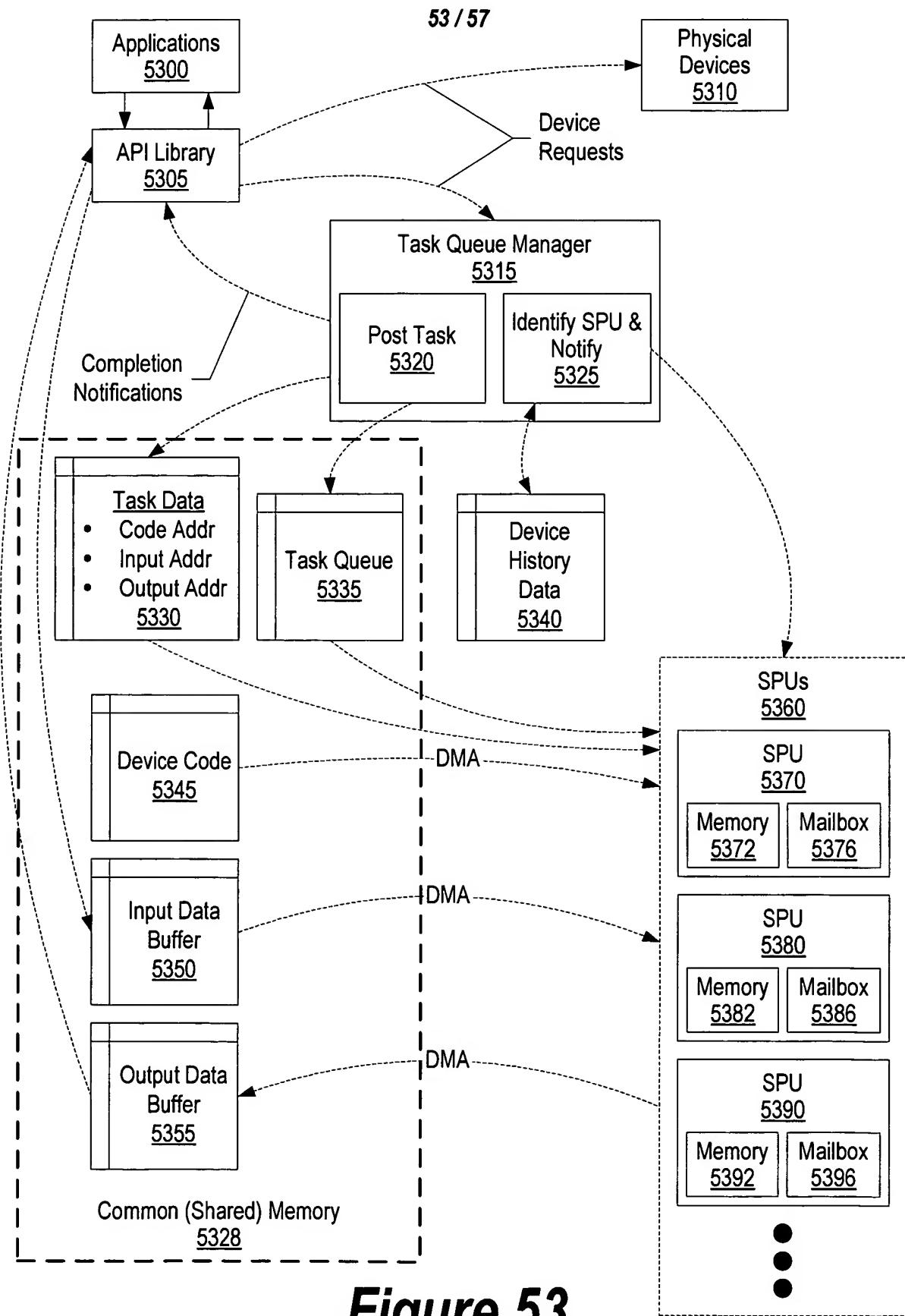


Figure 52



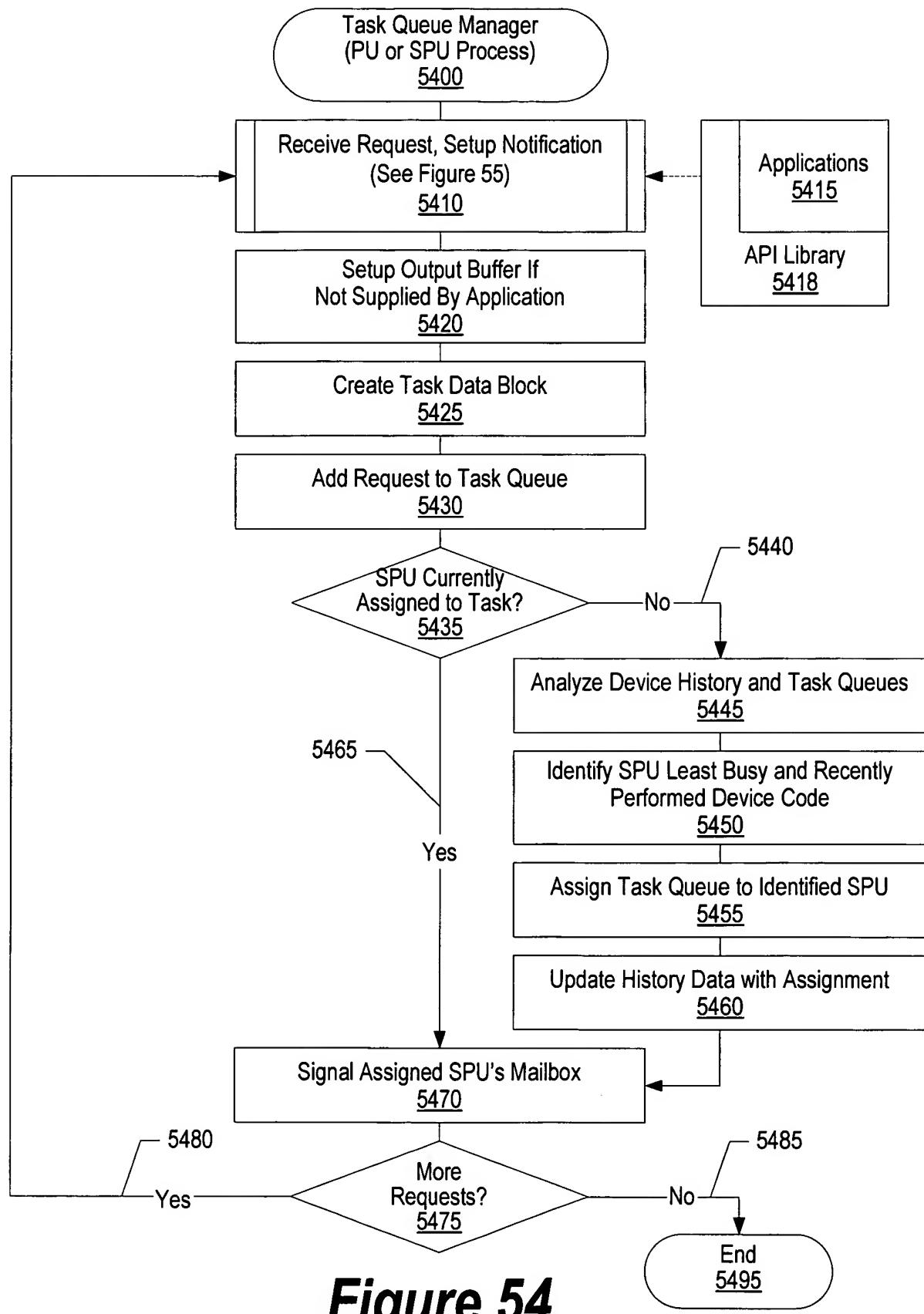


Figure 54

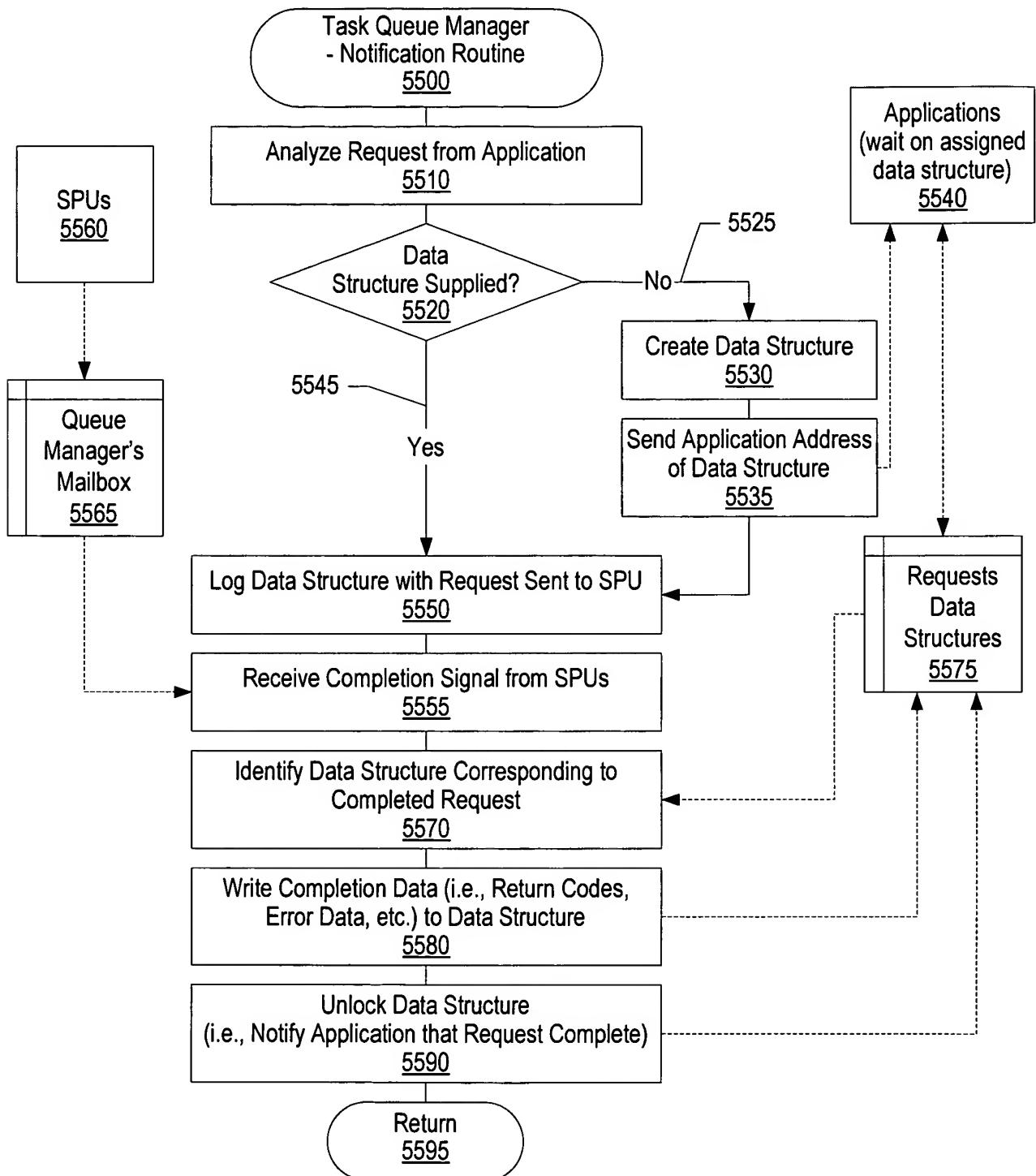
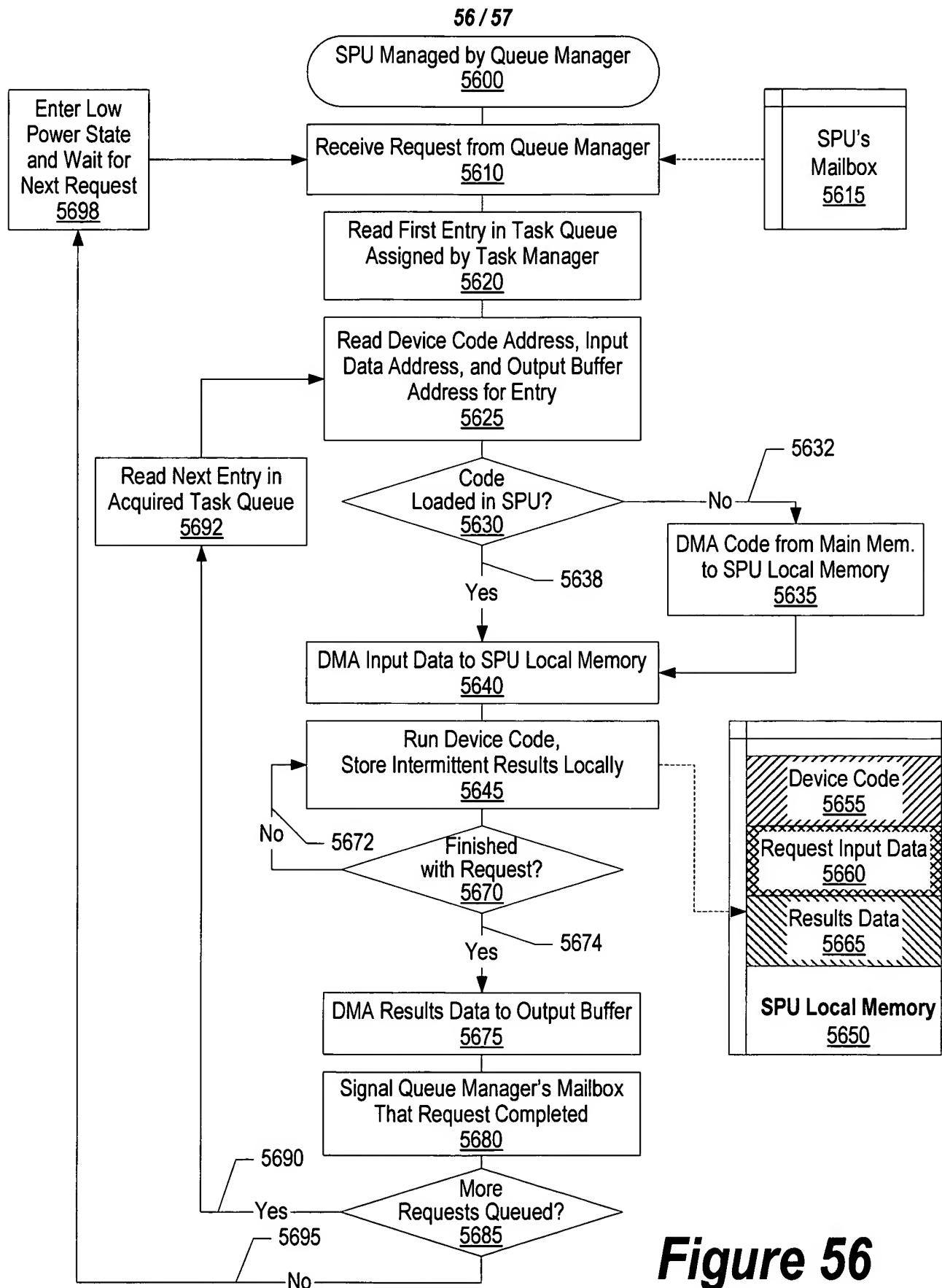


Figure 55

**Figure 56**

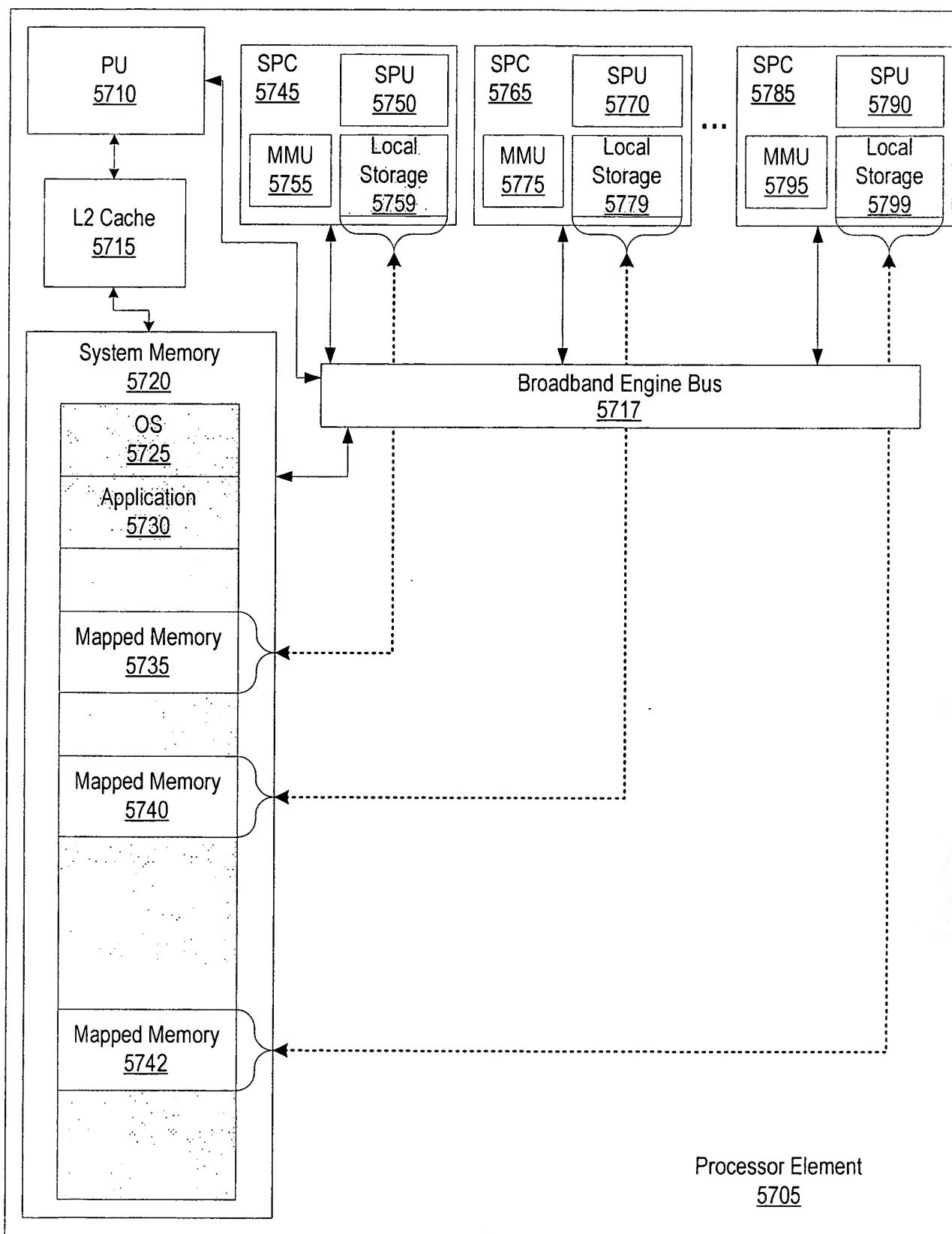


Figure 57